

# **SPECIFICATIONS**

CUSTOMER	_

# SAMPLE CODE : GFG128064I-YPFE-05

# DRAWING NO. : \_\_\_\_\_

# DATE : <u>2011.04.29</u>

# CERTIFICATION : ROHS

Customer Sign	Sales Sign	Approved By	Prepared By

### **Revision Record**

Data(y/m/d) 2011.04.29	Ver.	Description	Note	page
2011.04.29	00	New		17

		Quality Certified ISO 9001-2008 Licement 17 17 17 17 17 17 17 17 17 17 17 17 17

#### **CONTENTS**

1.	SCO	PE	 4
2.	PRO	DUCT SPECIFICATIONS	 4
	2.1	General	 4
	2.2	Mechanical Characteristics	 4
	2.3	Absolute Maximum Ratings	 5
	2.4	Electrical Characteristics	 5
	2.5	Optical Characteristics Absolute maximum ratings	 5
	2.6	Optical Characteristics	 6
	2.7	LED Back-light Characteristics	 7
3.	REL	IABILITY	 8
4.	OPE	RATING INSTRUCTIONS	 9

	4.1	Input signal Function	Qual ISO Licentre	ty Certified 9001:2008	Environmentally Certified ISQ 44001:2004 Limper Control Hope Coc.ec
	4.2	Voltage Generator Circuit		11	
	4.3	Timing Diagram		13	
5.	NOT	ΈS		16	
6.	OPE	RATION PRECAUTIONS		16	
7.	LCN	1 DIMENSIONS		17	

# 1. SCOPE

This specification covers the engineering requirements for the GFG128064I-YPFE-05 liquid crystal module.

# 2. PRODUCT SPECIFICATIONS

#### 2.1 General

- 128 \$64 dot matrix LCD
- STN (Y/G), Positive mode LCD panel
- Transflective, Wide temperature type
- 6 o'clock
- Back light: Edge LED (white)
- Multiplexing driving : 1/65duty, 1/9bias

Item	Characteristic
Dot configuration	128 �64
Dot dimensions(mm)	0.48 \$0.48
Dot spacing (mm)	0.52 \$0.52
Module dimensions (Horizontal Vertical & Thickness, mm)	80 �54 �9.7 max.
Viewing area (Horizontal Vertical, mm)	70.7 \$38.8
Active area (Horizontal &Vertical, GE <sup>139</sup> 78)	66.52 \$33.24

- Conteroller IC ST7565
- 2.2 Mechanical Characteristics



### 2.3 Absolute Maximum Ratings (Without LED back-light)

Characteristic	Symbol	Unit	Value
Operating Voltage (logic)	V <sub>DD</sub>	V	-0.3 to +5.0
Input Voltage	V <sub>IN</sub>	V	-0.3 to V <sub>DD</sub> +0.3

Note 1: Referenced to V<sub>SS</sub>=0V

### 2.4 Electrical Characteristics (Without LED back-light)

Characteristic	Symbol	Condition	Min.	Тур.	Max.	Unit
Operating Voltage(logic)	V <sub>DD</sub> -V <sub>SS</sub>		3.0	3.3	3.6	V
Input Voltage	V <sub>IH</sub>		0.8V <sub>DD</sub>		V <sub>DD</sub>	V
	VIL		V <sub>ss</sub>		0.2V <sub>DD</sub>	
Output Voltage	V <sub>OH</sub>	I <sub>он</sub> =-0.1mА	0.8V <sub>DD</sub>		V <sub>DD</sub>	V
	V <sub>HL</sub>	I <sub>OL</sub> =0.1mA	V <sub>ss</sub>		0.2V <sub>DD</sub>	
Current Consumption	I <sub>DD</sub>	V <sub>IN</sub> =V <sub>DD</sub>		0.05	1	mA

2.5 Optical Characteristics Absolute maximum ratings

Item	Symbol	Rating	Unit
Operating temperature range	Тор	-20~70	<b>⊕</b> C
Storage temperature range	Tst	-30~80	<b>⊕</b> C



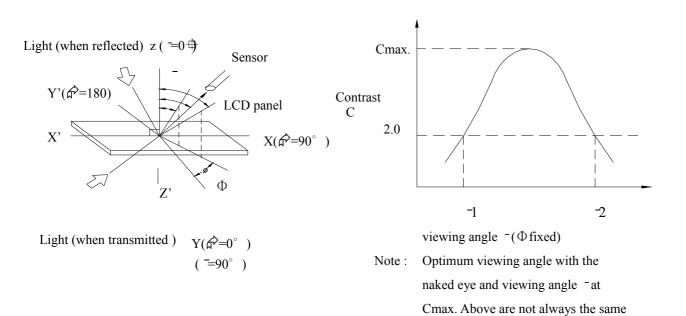
### 2.6 Optical Characteristics

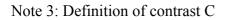
	1	705 duty,	17901as, v	op 10.0 <b>v</b> ,	1a-23 C	
Item	Symbol	Conditions	Min.	Тур.	Max	Reference
Driving voltage	Vop=VDD-VO		9.8	10.0	10.2	
Viewing angle	_	C≥2.0,¢>=0€€	30⊕	-		Notes 1 & 2
Contrast	С	-=5⊕☆=0⊕	3.0		-	Note 3
Response time(rise)	ton	-=5⊕☆=0⊕	-		198ms	Note 4
Response time(fall)	toff	-=5⊕☆=0⊕	-	-	176ms	Note 4

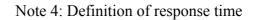
1/65 duty, 1/9bias, Vop=10.0V, Ta=25°C

Note 1: Definition of angles  $\neg$  and  $\cancel{P}$ 

Note 2: Definition of viewing angles  $\neg 1$  and  $\cancel{c}^2$ 



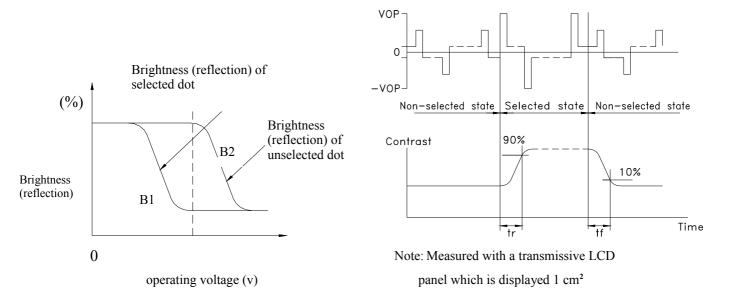




Brightness (reflection) of unselected dot (B2)



Brightness (reflection) of selected dot (B1)





V OPR : Operating voltage f <sub>FRM</sub> : Frame frequency t<sub>ON</sub> : Response time (rise)

t <sub>OFF</sub> : Response time (fall)

### 2.7 LED Back-light Characteristics

#### 2.7.1 Electrical / optical specifications

	$Ta = 25 \oplus C$					
Item	Symbol	Condition	Min.	Тур.	Max.	Unit
Forward voltage	$V_{\mathrm{f}}$	If=60mA, White	2.9	3.2	3.6	V
LED *Luminous Intensity	Iv	If=60mA, White		150		Cd/m2
Chromaticity Coordinate	Х	If=60mA, White	0.26	0.31	0.36	
	у		0.25	0.32	0.37	
Reverse Current	$I_R$	VR=5V, White			0.1	mA

Note: \* Measured at the bare LED back-light unit.

### 2.7.2 LED Maximum Operating Range

Item	Symbol	White	Unit	
Power Dissipation	$P_{AD}$	288	mW	
Forward Current	$I_F$	80	mA	
Reverse Voltage	V <sub>R</sub>	5	V	



# **3. RELIABILITY**

### 3.1 Reliability

Test item	Test condition	Evaluation and assessment
Operation at high temperature and humidity	40 °C ⊕2 °C 90%RH for 500hours	No abnormalities in functions* and appearance**
Operation at high temperature	60 °C ⊕2 °C for 500 hours	No abnormalities in functions* and appearance**
Heat shock	-20 ↔~ +60 °C Left for 1 hour at each temperature, transition time 5 min, repeated 10times	No abnormalities in functions* and appearance**
Low temperature	-20 € °C for 500 hours	No abnormalities in functions* and appearance**
Vibration	Sweep for 1 min at 10 Hz, 55Hz, 10Hz, amplitude 1.5mm 2 hrs each in the X,Y and Z directions	No abnormalities in functions* and appearance**
Drop shock	Dropped onto a board from a height of 10cm	No abnormalities in functions* and appearance**

\* Dissipation current, contrast and display functions

\*\* Polarizing filter deterioration, other appearance defects

### 3.2 Liquid crystal panel service life

100,000 hours minimum at 25 °C +10 °C

- 3.3 definition of panel service life
  - Contrast becomes 30% of initial value
  - Current consumption becomes three times higher than initial value
  - Remarkable alignment deterioration occurs in LCD cell layer
  - Unusual operation occurs in display functions



# 4. OPERATING INSTRUCTIONS

### 4.1 Input signal Function

Pin No	Symbol	I/O	Function
1	/CS1	I	This is the chip select signal. When CS1 = "L" and CS2 = "H," then the
			chip select becomes active, and data/command I/O is enabled.
2	/RES	I	When RES is set to "L," the settings are initialized. The reset operation is
			performed by the RES signal level.
3	A0	I	This is connect to the least significant bit of the normal MPU address bus,
			and it determines whether the data bits are data or a command.
			A0 = "H": Indicates that D0 to D7 are display data.
			A0 = "L": Indicates that D0 to D7 are control data.
4	WR(R/W)	I	<ul> <li>When connected to an 8080 MPU, this is active LOW.</li> </ul>
			(R/W) This terminal connects to the 8080 MPU WR signal. The signals on
			the data bus are latched at the rising edge of the WR signal.
			When connected to a 6800 Series MPU:
			This is the read/write control signal input terminal.
			When R/W = "H": Read. When R/W = "L": Write.
5	RD(E)	I	When connected to an 8080 MPU, this is active LOW.
			(E) This pin is connected to the RD signal of the 8080 MPU, and the
			ST7565S series data bus is in an output status when this signal is "L".
			When connected to a 6800 Series MPU, this is active HIGH.
			This is the 6800 Series MPU enable clock input terminal.
6~13	D0 to D5	I/O	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit
	D6 (SCL)		standard MPU data bus. When the serial interface is selected (P/S = "L") :
	D7 (SI)		D0 to D5 are set to high impedance.
			D6 : the serial clock input (SCL) ; D7 : serial data input (SI) .
			When the chip select is not active, D0 to D7 are set to high impedance.
14	VDD	PS	Shared with the MPU power supply terminal Vcc.
15	VSS	PS	This is a 0V terminal connected to the system GND.
16	VOUT	0	DC/DC voltage converter. Connect a capacitor between this terminal and
			VSS.
17	CAP5-	0	DC/DC voltage converter. Connect a capacitor between this terminal and
			the CAP1+ terminal.
18	CAP3-	0	DC/DC voltage converter. Connect a capacitor between this terminal and
			the CAP1+ terminal.
19	CAP1+	0	DC/DC voltage converter. Connect a capacitor between this terminal and
			the CAP1- terminal.
20	CAP1-	0	DC/DC voltage converter. Connect a capacitor between this terminal and
			the CAP1+ terminal.

							Quality Certified ISO 9001-2008 Licen <b>TOCSI</b> C-E	Environmentally Certifie ISQ 14001:2004			
21	CAP2-	0	DC/D	C voltage conver	ter. Conne	ct a capacitor	between this t	erminal and			
			the C	ne CAP2+ terminal.							
22	CAP2+	0	DC/D	C/DC voltage converter. Connect a capacitor between this terminal and							
			the C	AP2- terminal.							
23	CAP4-	0		C voltage conver AP2+ terminal.	ter. Conne	ct a capacitor	between this t	erminal and			
24	VRS	PS	This is	his is the internal-output VREG power supply for the LCD power supply							
				, je regulator.		,	·				
25~29	V1,V2,	PS		s a multi-level po	ower supply	for the liquid	d crystal drive.	The voltage			
	V3,V4, V5			y applied is dete		•	5	ů l			
				gh the use of a	-	-	-	_			
				ance using an		U U	•	00			
				and must mainta		C					
			relativ	e magnitudes sh	own below.						
			VDD	(= V0) ≧V1 ≧V2	≧V3 ≧V4	$k \ge V5$					
30	VR	I	Outpu	it voltage regulate	or terminal.	Provides the	voltage betwee	n VDD and			
			V5 th	V5 through a resistive voltage divider.							
			IRS =	"L" : the V5 volta	ge regulato	or internal resi	stors are not us	ed.			
			IRS =	"H" : the V5 volta	age regulate	or internal resi	stors are used				
31	C86	I	This is	s the MPU interfa	ce switch te	erminal.					
			C86 =	"H": 6800 Series	MPU inter	face. C86 = '	"L": 8080 MPU	interface.			
32	P/S	I	This is	s the parallel data	a input/seria	al data input sv	witch terminal.				
			P/S =	"H": Parallel data	input. P/	′S = "L": Seria	l data input.				
			The fo	ollowing applies d	epending c	on the P/S stat	tus:				
			P/S	Data/Comman	Data	Read/Write	Serial Clock				
			"	A0	D0 to D7	RD, WR	X				
			H"								
			"L "	A0	SI (D7)	Write only	SCL (D6)				
			When	P/S = "L", D0 to	D5 may be	"H", "L" or Op	ben.	1			
			RD (E	and WR (R/W)	are fixed to	either "H" or	"L".				
			· ·	serial data input, l							
33	/HPM	I		s the power con	•			uit for liquid			
				ıl drive. /HPM = "l		•					
34	IRS	I	This t	erminal selects th	e resistors	for the V5 vol	tage level adjus	stment.			
				"H": Use the inte			-				
			IRS =	"L": Do not use t	he internal	resistors. The	V5 voltage leve	el is			
			regula	ated by an exte	rnal resisti	ve voltage di	ivider attached	to the VR			
			termir								

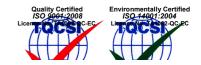


Table 1

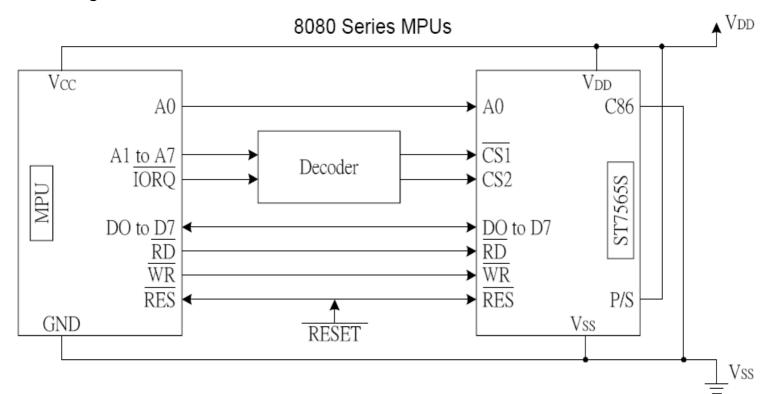
P/S	/CS1	CS2	<b>A</b> 0	/RD	/WR	C86	D7	D6	D5~D0
H: Parallel Input	/CS1	CS2	A0	/RD	/WR	C86	D7	D6	D5~D0
L: Serial Input	/CS1	CS2	A0	-	—	-	SI	SCL	(HZ)
" "indicate	- Europhan	Ala a v 61 12 a v	4 - 61 2						

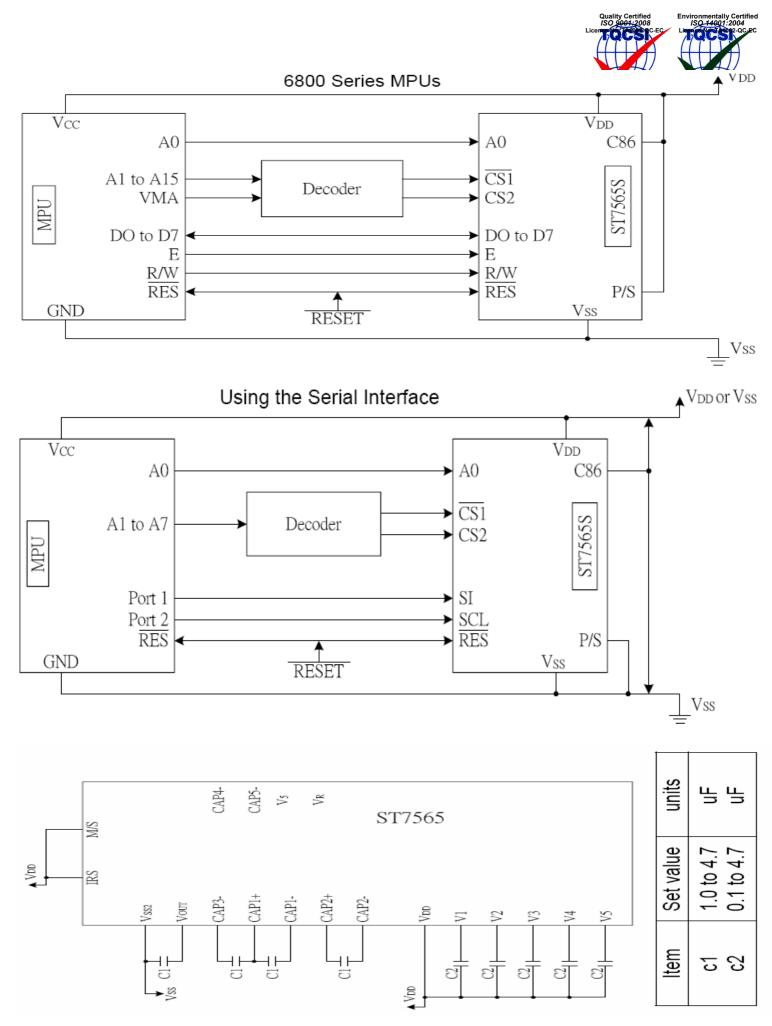
—" indicates fixed to either "H" or to "L"

Table 2										
C86 (P/S=H) /CS1 CS2 A0 E(/RD) R/W(/WR) D7~D0										
H: 6800 Series	/CS1	CS2	A0	E	R/W	D7~D0				
L: 8080 Series	/CS1	CS2	A0	/RD	/WR	D7~D0				

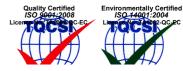
Shared	6800 Series	8080 \$	Series	Eurotion	
A0	R/W	/RD	/WR	Function	
1	1	0	1	Reads the display data	
1	0	1	0	Writes the display data	
0	1	0	1	Status read	
0	0	1	0	Write control data (command)	

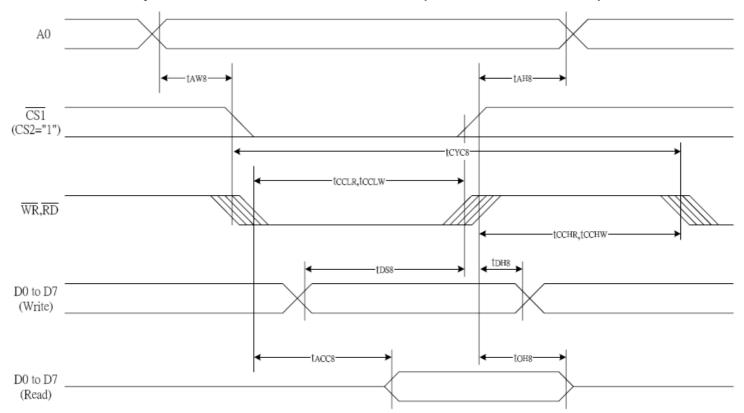
### 4.2 Voltage Generator Circuit





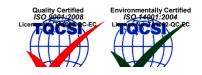
### 4.3 Timing Diagram

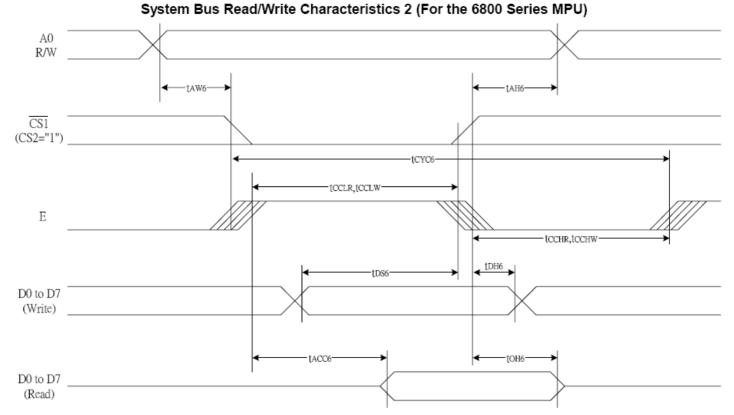




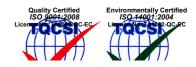
System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)

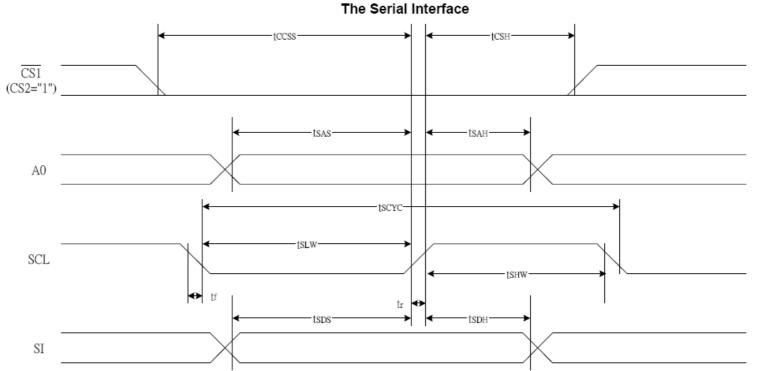
Item	Signal	Symbol	Condition	Rat	Rating	
				Min	Max.	
Address hold time	A0	t <sub>AH8</sub>		0		ns
Address setup time		t <sub>AW8</sub>		0		ns
System cycle time	A0	t <sub>CYC8</sub>		240		
Control L pulse width (WR)	WR	$t_{\text{CCLW}}$		80		ns
Control L pulse width (RD)	RD	t <sub>CCLR</sub>		140		ns
Control H pulse width (WR)	WR	t <sub>CCHW</sub>		80		ns
Control H pulse width (RD)	RD	t <sub>CCHR</sub>		80		ns
RD access time	D0 to	t <sub>DS8</sub>		40		ns
Output disable time	D7	t <sub>DH8</sub>		10		ns
		t <sub>ACC8</sub>	C <sub>L</sub> =100pF		70	ns
		t <sub>OH8</sub>		5	50	ns





Condition Item Signal Symbol Rating Units Min Max. Address hold time A0 0 - $t_{\rm AH8}$ -ns Address setup time 0  $t_{AW8}$ -ns System cycle time A0 240  $t_{CYC8}$ --WR Control L pulse width (WR) 80 ---ns  $t_{\text{CCLW}}$ Control L pulse width (RD) RD 140  $t_{\text{CCLR}}$ ns --Control H pulse width (WR) WR 80  $t_{\rm CCHW}$ -ns Control H pulse width (RD) RD 80 ns t<sub>CCHR</sub> --RD access time D0 to 40  $t_{\rm DS8}$ ns ----D7 Output disable time 10 -ns  $t_{\rm DH8}$ C<sub>L</sub>=100pF 70  $t_{ACC8}$ --ns 5 50 ns  $t_{\rm OH8}$ 





Item	Signal	Symbol	Condition	Rating		Units
				Min	Max.	
Serial Clock Period	SCL	Тѕсус		50		ns
SCL "H" pulse width		Tshw		25		ns
SCL "L" pulse width		TSLW		25		ns
Address setup time	A0	TSAS		20		ns
Address hold time		Tsah		10		ns
Data setup time	SI	Tsds		20		ns
Data hold time		TSDH		10		ns
CS-SCL time	CS	Tcss		20		ns
CS-SCL time		Tcsh		40		ns

# 5. NOTES

Safety PAGE 14/16



• If the LCD panel breaks, be careful not to get the liquid crystal in your mouth. If the your skin or clothes, wash it off immediately using soap and plenty of water.

### <u>Handling</u>

- Avoid static electricity as this can damage the CMOS LSI.
- The LCD panel is plate glass; do not hit or crush it.
- Do not remove the panel or frame from the module.
- The polarizing plate of the display is very fragile; handle it very carefully

### Mounting and Design

- Mount the module by using the specified mounting part and holes.
- To protect the module from external pressure, leave a small gap by placing transparent plates (e.g. acrylic or glass ) on the display surface, frame, and polarizing plate
- Design the system so that no input signal is given unless the power-supply voltage is applied.
- Keep the module dry. Avoid condensation, otherwise the transparent electrodes may break.

#### Storage

- Store the module in a dark place where the temperature is 25 °C +10 °C and the humidity below 65% RH.
- Do not store the module near organic solvents or corrosive gases.
- Do not crush, shake, or jolt the module (including accessories).

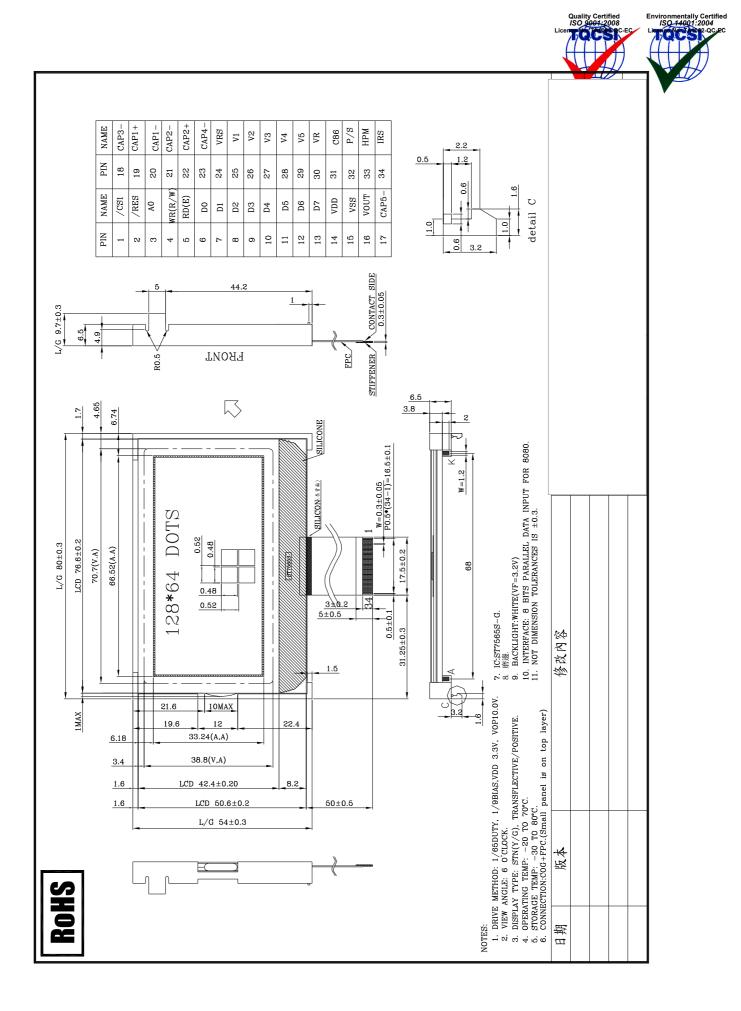
### Cleaning

- Do not wipe the polarizing plate with a dry cloth, as it may scratch the surface.
- Wipe the module gently with soft cloth soaked with a petroleum benzine.
- Do not use ketonic solvents (ketone and acetoe) or aromatic solvents (toluene and xylene), as they may damage the polarizing plate.

# 6. OPERATION PRECAUTIONS

Any changes that need to be made in this specification or any problems arising from it will be dealt with quickly by discussion between both companies.

### 7. LCM Dimension



PAGE 16/16