SPECIFICATIONS

CUSTOMER : _____

SAMPLE CODE : GFT057GA320240Y

DRAWING NO. : _____

DATE : 2008.11.11

CERTIFICATION : ROHS

Customer Sign	Sales Sign	Approved By	Prepared By

Revision Record

Data(y/m/d)	Ver.	Description	Note	page
2008.11.11	00	New		28

2009.06.16	01	Add CONNECT DRAWING		**27**

CONETNTS

1. SUMMARY

This technical specification applies to 5.7“ color TFT-LCD panel with touch panel.
The 5.7“ color TFT-LCD panel is designed for industry, vehicle application and other electronic products which require high quality flat panel displays.

2. FEATURES

High Resolution: 230,400 Dots (320 RGB X 240). Image Reversion: Up/Down and Left/Right.

3. GENERAL SPECIFICATIONS

Parameter		Specifications	Unit
Screen Size		5.7(Diagonal)	inch
Display Format		320 RGB x 240	Dot
Active Area		115.20(H) x 86.40(V)	mm
Dot pitch		0.12(H) x 0.36(V)	mm
Surface treatment		Anti-glare	
Pixel Configuration		RGB-Stripe	
Outline Dimension		126.00(W) x 101.55(H) x 7.4(D)	mm
Weight		(100)	g
View Angle Direction		6 o’clock	
Temperature Range	Operation	-10~60	°C
	Storage	-20~70	°C

4. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Values		Unit	Condition
		Min.	Max.		
Power Voltage	V_{DD} ,VCC	-0.3	7	V	GND=0
	V_{GH}	-0.3	32	V	GND=0

	V_{GL}	-22	0.3	V	GND=0
	$V_{GH}-V_{GL}$	-0.3	+45	V	GND=0
Input Signal Voltage	V_{in}	-0.3	V_{DD}+0.3	V	GND=0
Logic Output Voltage	V_{OUT}	-0.3	+0.7	V	GND=0

Note : Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above

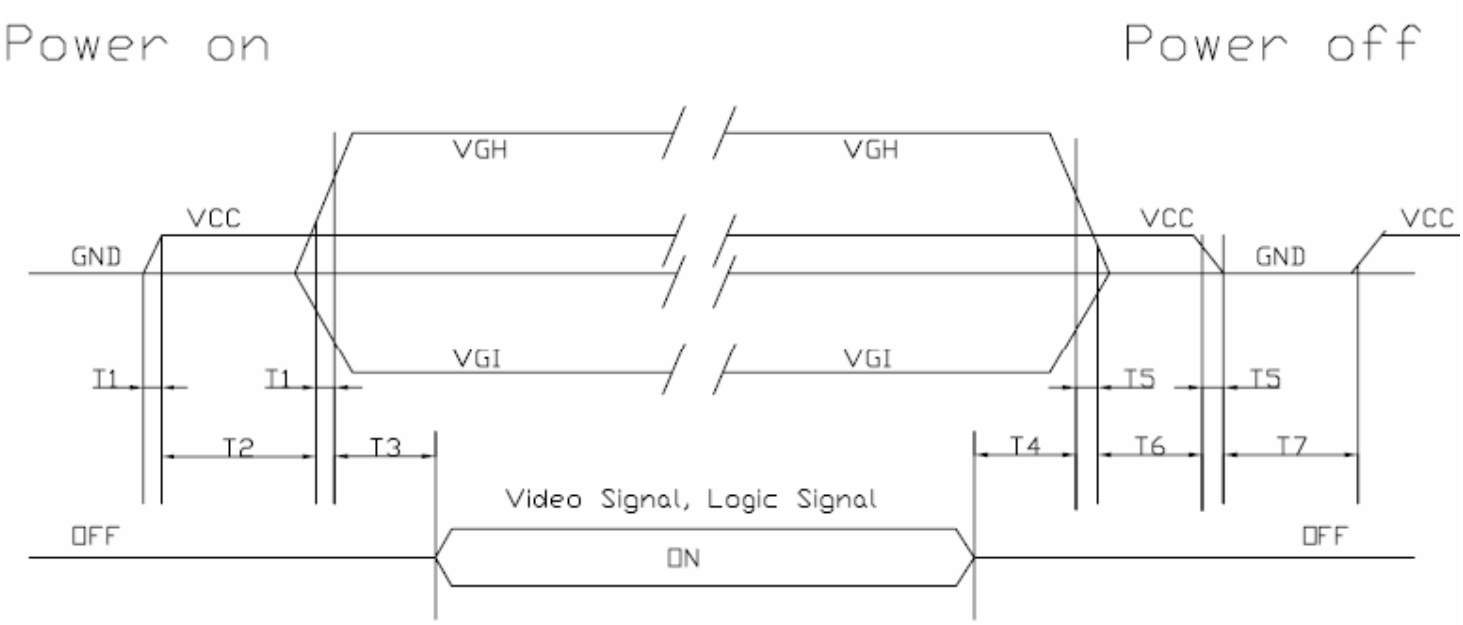
5. ELECTRICAL CHARACTERISTICS

5.1 Operating conditions:

Item	Symbol	Rating			Unit	Remark
		Min.	Typ.	Max.		
Power Voltage	VCC	3.0	3.3	3.6	V	
	VDD	3.8	5.0	5.5	V	
	VGH	10	-	30	V	
	VGL	-17	-	-5	V	
Low level input voltage	VIL	0	-	0.3 VDD	V	SPCL, SPDA,UD,LRC,IF1,IF2
Hight level input voltage	VIH	0.7 VDD	-	VDD	V	
Analog operating current	IAVDD	-	-	TBD	mA	f_{CLKIN}=27MHz,f_{OEH}=15.7KHz, VDDA=5V

5.2 Power Sequence

Sequence for power on/off and Signal on/off



T1≤ 15ms(From 10% VCC to 90%*VCC, when VCC is Low to High) ;
T2 ≤10ms(From 90% VCC to 10%*VCC, when VCC is Low to High) ;
T3 ≤10ms(From 90% VGH to Video signal, when VGH is Low to High) ;
T4 ≤10ms(From Video signal to 90%*VGH,, when VGH is High to Low) ;
T5 ≤20ms(From 90% VCC to 10%*VCC, when VCC is High to Low) ;
T6≤10ms(From 10% VGH to 90%*VCC, when VCC is Low to High) ;
T7≤0.4s(From 10% VCC is H→Lto 10%*VCC is L→H)

To prevent the device from damage due to latch-up, the power ON/OFF sequence shown below must be followed.

Power ON : VDD, VCC → VGL → Input Signals → VGH

Power OFF : VGH → Input Signals → VGL → VDD, VCC

5.3 LED driving conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
LED current	-	-	140	-	mA	Note 1
LED voltage	V_{LED1},V_{LED2},V_{LED3},V_{LED4}	9.9	-	10.5	V	
LED Life Time	-	(10,000)	-	-	Hr	Note 2,3

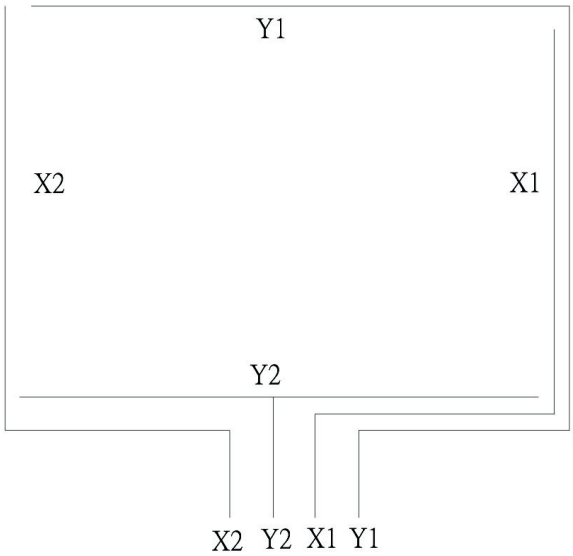
Note 1 : There are 4 Groups LED , $V_{LED1,2,3,4}$=9.9 V (min.)

Note 2 : Ta = 25℃ ,

Note 3 : Brightess to be decreased to 50% of the initial value

6. TOUCH PANEL

6.1 Block diagram



6.2 Absolute maximun ratings

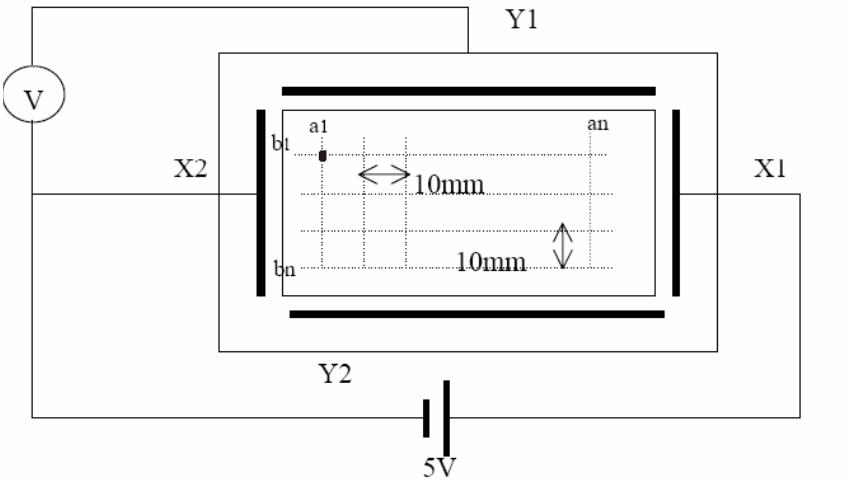
Item	Symbol	Condictions	Specifications	Unit
Supply voltage	-	-	DC 5.0	V

6.3 Electrical characteristics

Item	Symbol	Condictions	Min	Typ	Max	Unit	Note
Resistance between terminal	RX	-	200	460	900	ohm	Note1
	RY	-	200	350	900	Ohm	Note1
Insulation resistance	RINS	DC 25V	25	-	-	M ohm	Note1
Linearity (Note2,3)	-	-			1.5	%	Note1
Chattering	-	-			10max	ms	Note1

Note1.This specifications applied to only touch panel and calibration is more than 3 points.

Note 2.Test condiction



(a) X- axis linearity method V_{Y2}-V_{Y1}=5V, V_{OUT}=V_{X2}

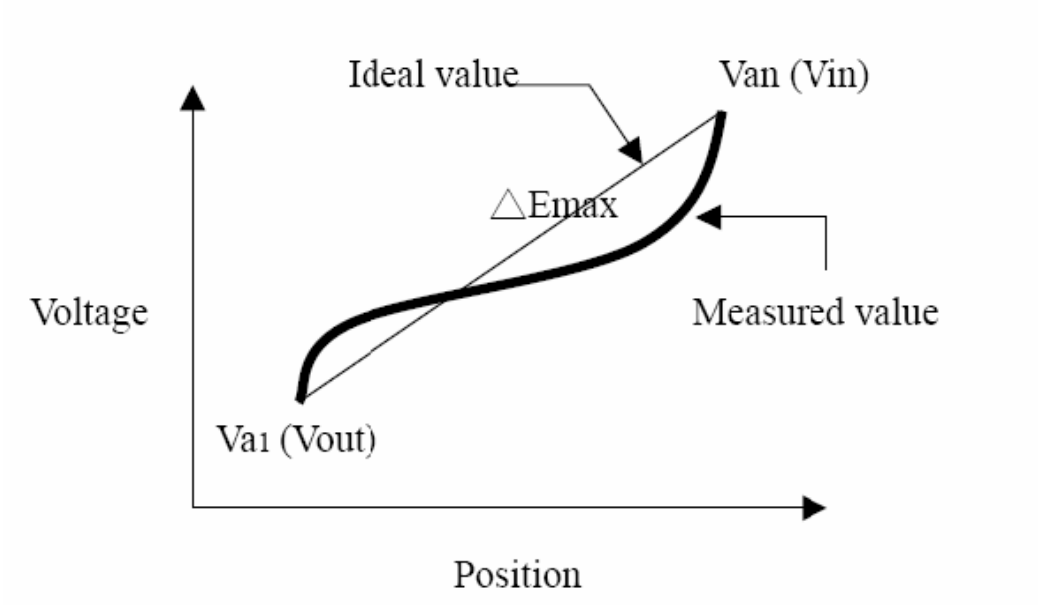
(b) Y- axis linearity method V_{x1}-V_{x2}=5V, V_{OUT}=V_{Y1}

Note 3.Calcutioon

Define linearity Xi as:

Linearity Xi= IΔE maxI /(Van-Val)

Linearity X=Max(Linearity x1,…..Linearity xn)



6.4 Mechanical characteristics

Item	Condiction	Specifications	Note
Operation force	pen (push vertically)	80g max	

	(Top R0.8, material polyacetal)		
	rubber (push vertically) (Top R8, material polyacetal)	130g max	
Hardness of surface	3H(JIS-K5400)	Pencil hardness 2hmin.	

7. AC Characteristics

7.1. CCIR601/656 Interface

7.1.1. Input signal characteristics

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
CLK period	T_{OSC}	-	37	-	ns
Data setup time	T_{SU}	12	-	-	ns
Data hold time	T_{HD}	12	-	-	ns

7.1.2 Hardware reset timing

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
RESET low pulse width	T_{RSB}	10	-	-	μs

7.1.3. Output signal characteristics

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
Rising time	T_r	-	-	10	ns
Falling time	T_f	-	-	10	ns
Internal STH setup time	T_{SUS}	12	-	-	ns
Internal STH hold time	T_{HDS}	12	-	-	ns
Internal data setup time	T_{SUD}	60	-	-	ns
Internal data hold time	T_{HDD}	40	-	-	ns
OEH pulse width	T_{OEH}	-	1248	-	ns
OEV pulse width	T_{OEV}	-	4996	-	ns
CKV pulse width	T_{CKV}	-	3744	-	ns
Hsync – DEH time	T1	-	4368	-	ns
Hsync – CKV time	T2	-	2496	-	ns
Hsync – OEV time	T3	-	624	-	ns

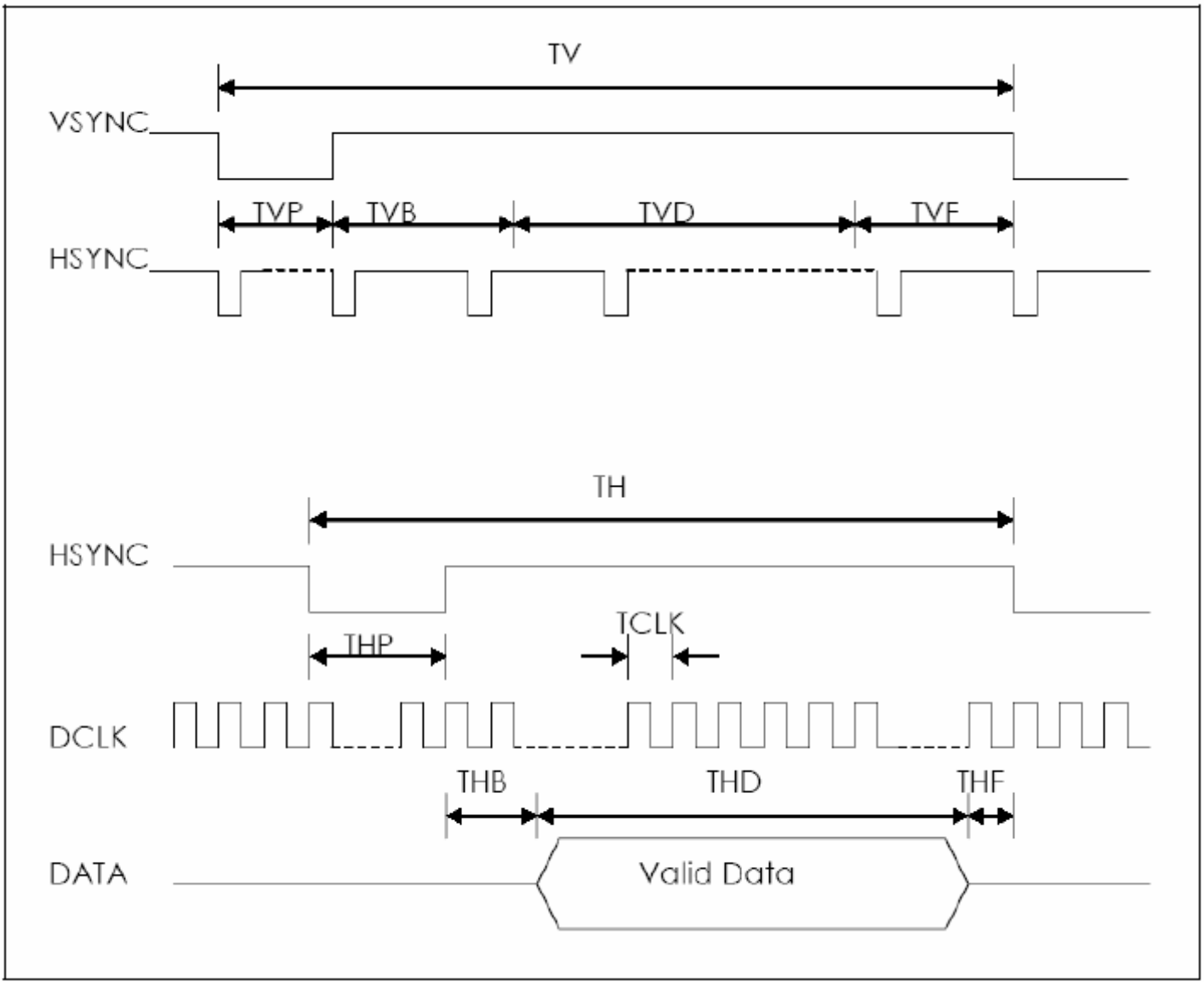
Vsync – setup time		T_{SUV}		1872	-	ns
Vsync – pulse time		T_{STV}		1	-	T_H
Vsync – STV time	NTSC	T_{VS1}	-	19	-	T_H
	PAL	T_{VS1}	-	27	-	T_H
OEH – STV time		T_{HE}	-	2	-	T_H
Output settling time		T_{OES}	-	12	20	μs

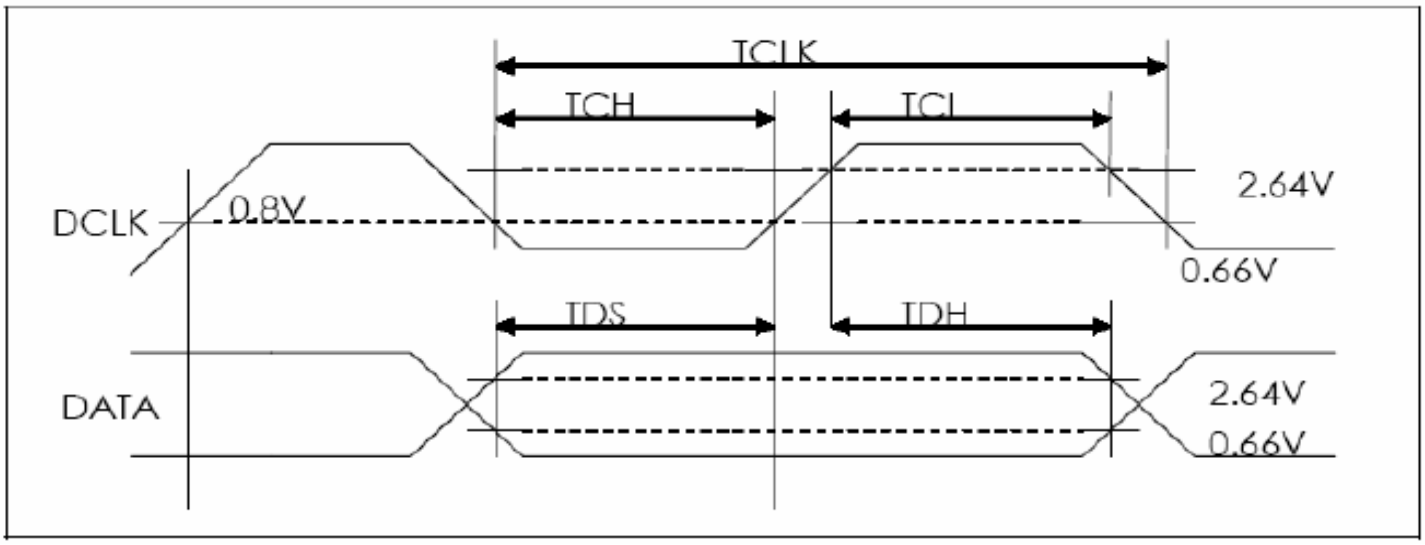
7.2. 24-bits parallel RGB Interface

7.2.1 AC Timing Characteristics

Signal	Item		Symbol	Min.	Typ.	Max.	Unit
Dclk	Frequency		Dclk	-	6.4	-	MHZ
	High Time		Tch	-	78	-	ns
	Low Time		Tcl	-	78	-	ns
Data	Setup Time		Tds	12		-	ns
	Hold Time		Tdh	12		-	ns
Hsync	Period		TH	-	408	-	DCLK
	Pulse Width		Thp	-	30	-	DCLK
	Back-Porch		Thb	-	38	-	DCLK
	Display Period		Thd	-	320	-	DCLK
	Front-Porch		Thf	-	20	-	DCLK
Vsync	Period	NTSC	Tv	-	262.5	-	TH
		PAL		-	312.5	-	
	Pulse Width		Tvp	1	3	5	TH
	Back-Porch	NTSC	Tvb	-	15	-	TH
		PAL		-	23	-	
	Display Period		Tvd	-	240	-	TH
	Front-Porch	NTSC	Tvf	-	4.5	-	TH
		PAL		-	46.5	-	

7.2.2 AC Timing Diagrams



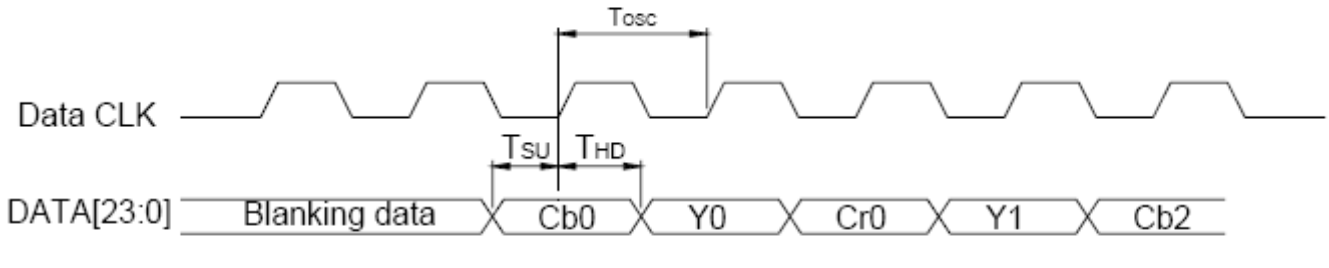


8. Waveform

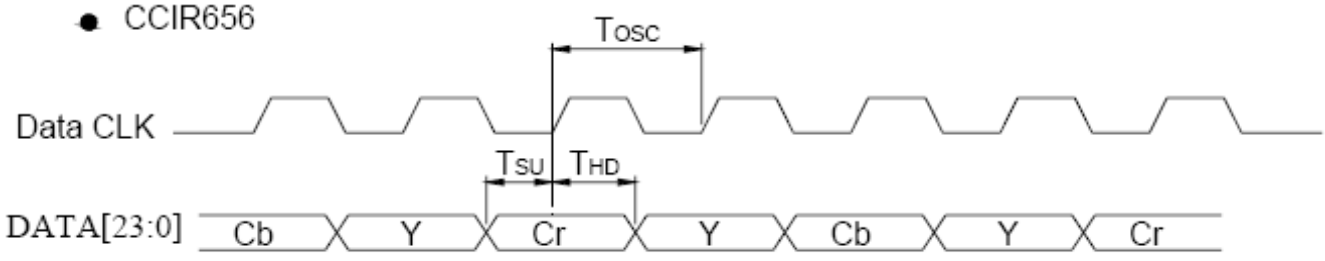
8.1. Timing Controller Timing Chart

8.1.1. Clock and Data waveform

- CCIR601(HS_POL="L" in Register R2)



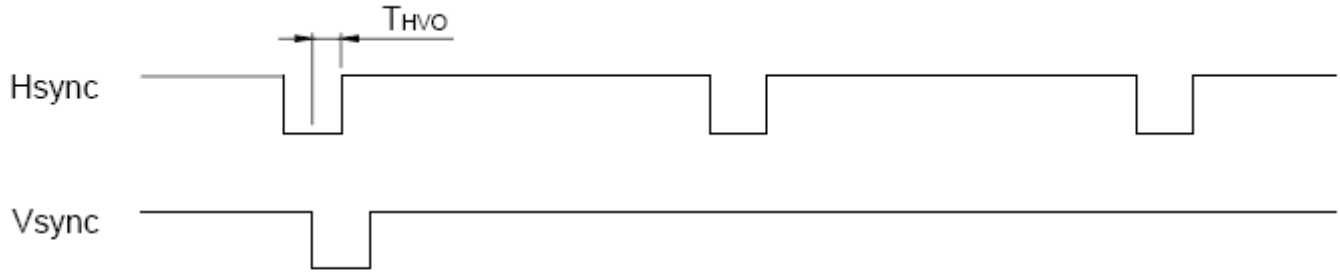
- CCIR656



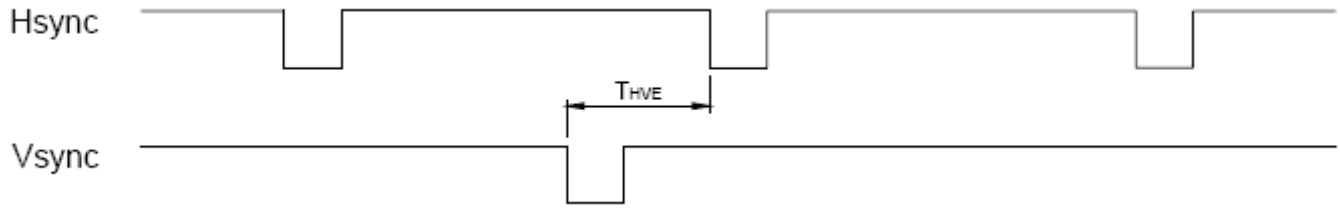
8.1.2 Digital / Analog RGB timing waveform

8.1.2.1 Hsync and Vsync timing

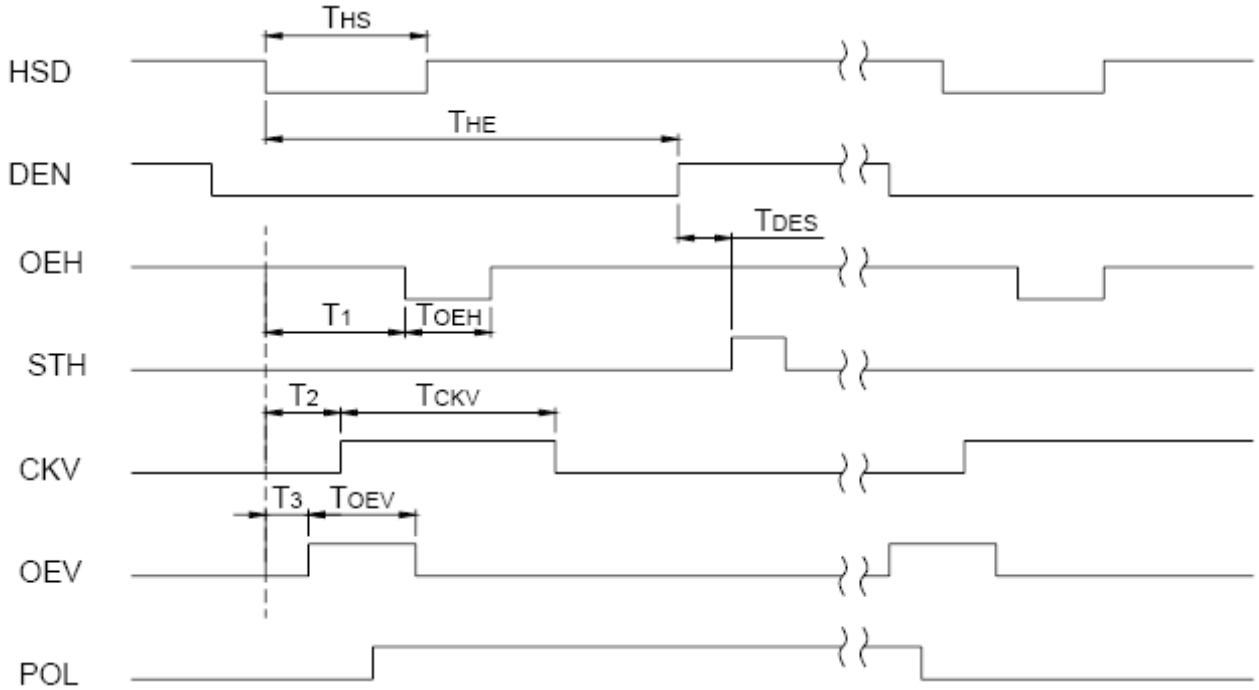
● Odd field



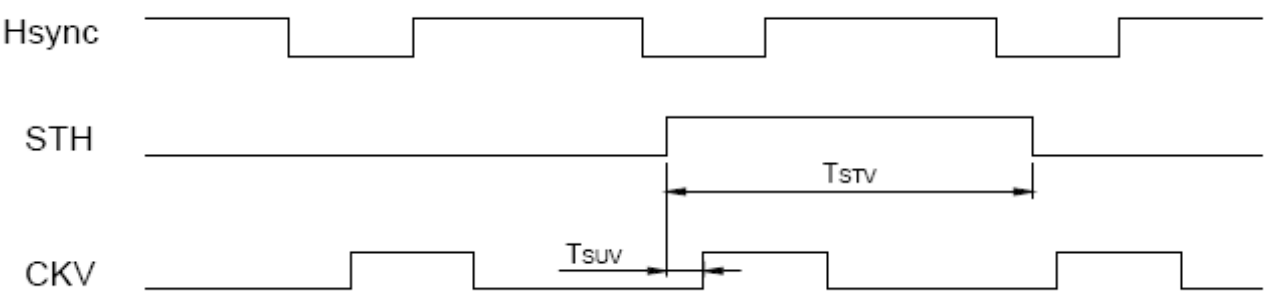
● Even field



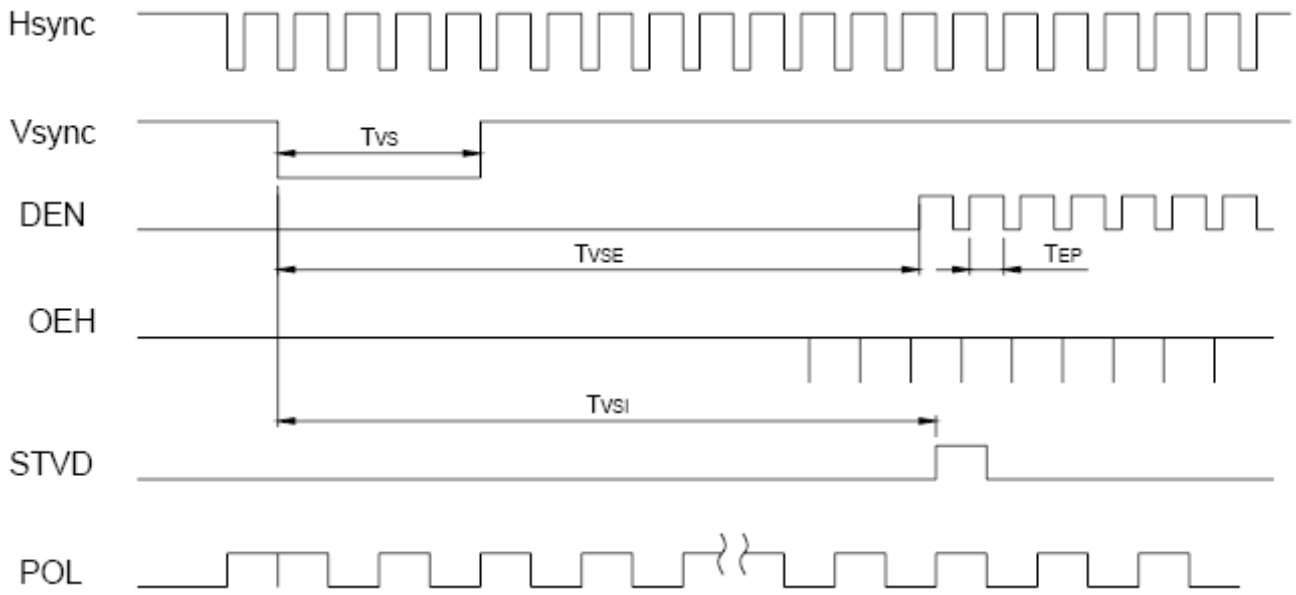
8.1.2.2 Hsync and horizontal control timing waveform



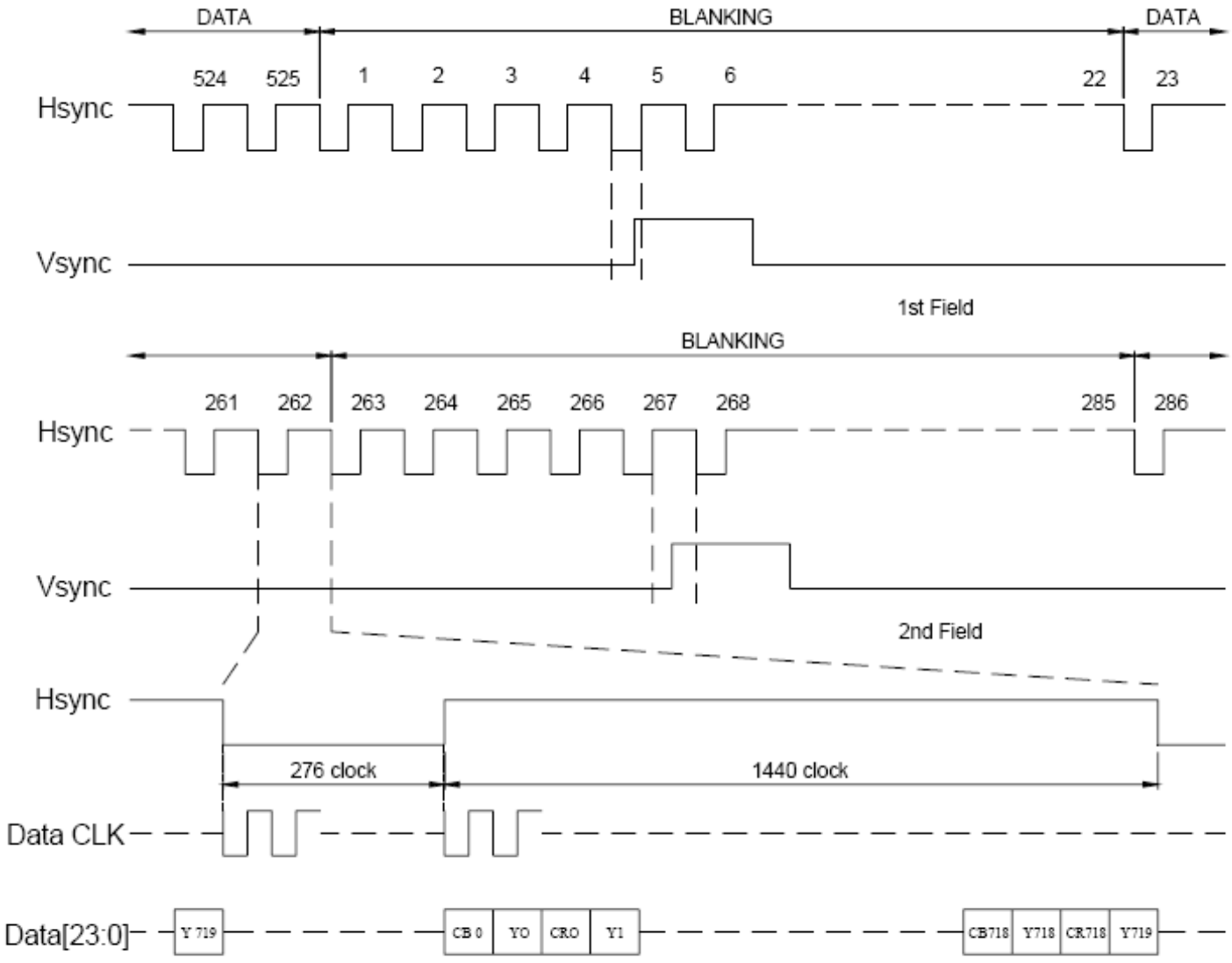
8.1.2.3 Hsync and vertical shift clock timing waveform



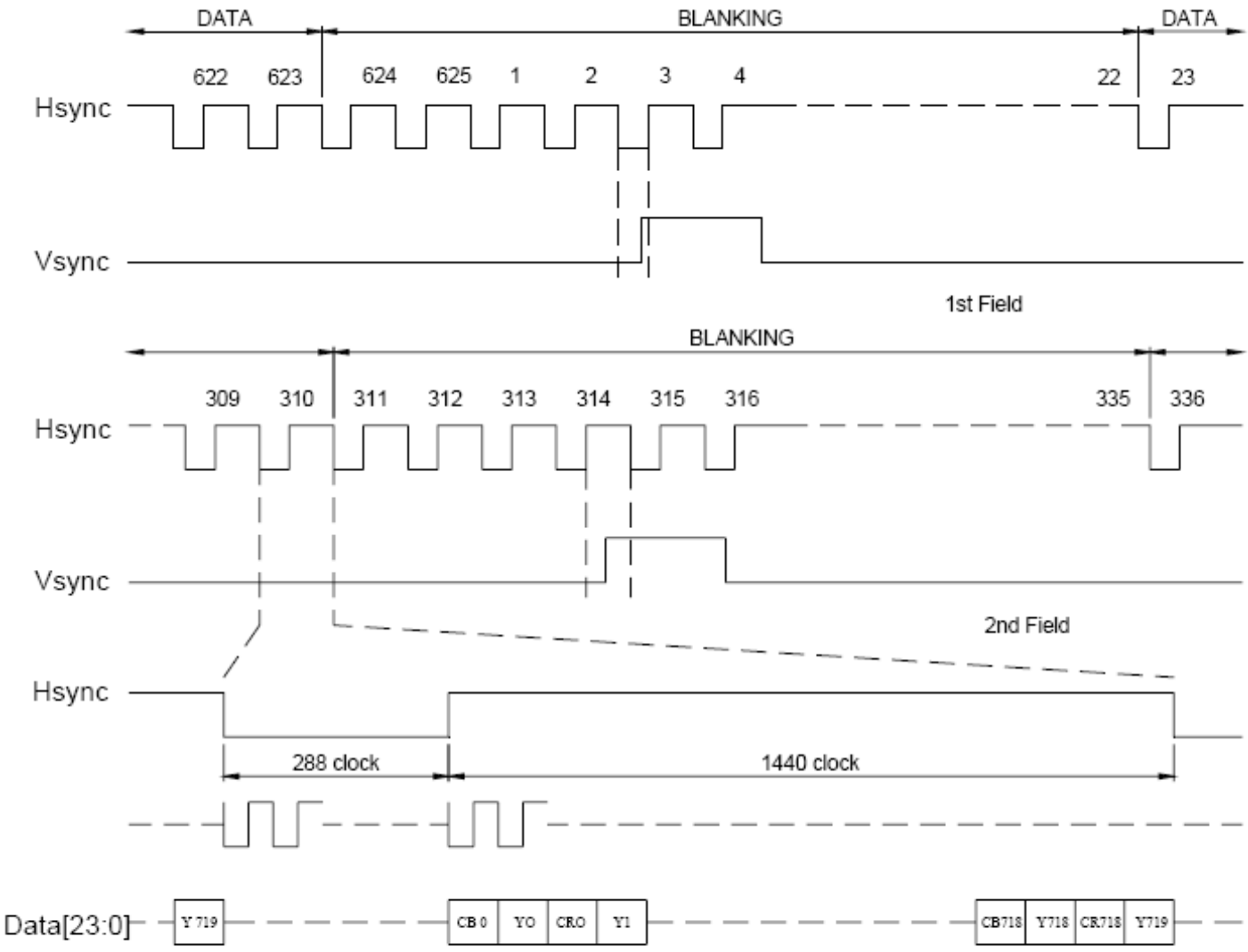
8.1.2.4 Hsync and vertical control timing waveform



8.1.3 CCIR601 timing waveform (VS_POL="H" , HS_POL="L" in Register R2)



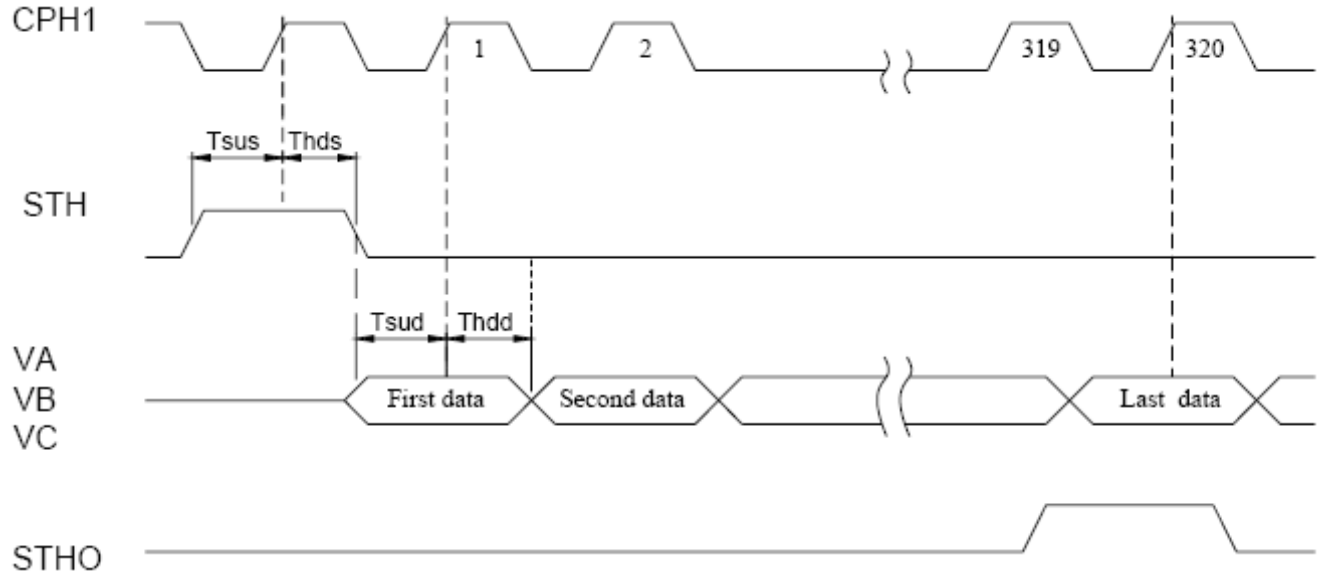
ITU-BT.601 NTSC Input Timing



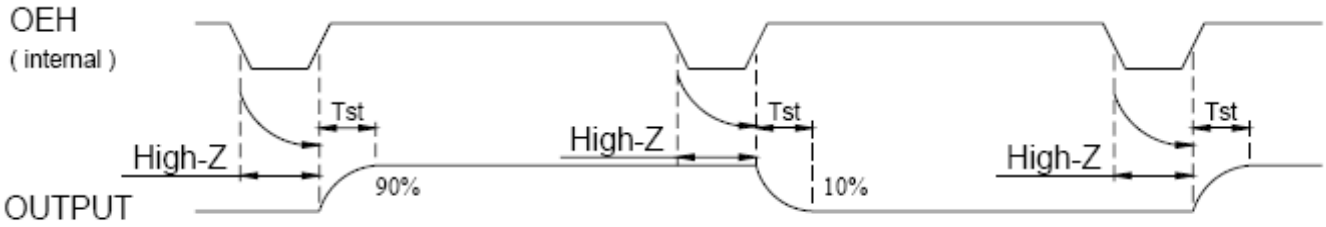
ITU-BT.601 PAL Input Timing

8.2 Source Driver Timing Chart

8.2.1 Clock and Start Pulse timing waveform



8.2.2 OEH and Data Output timing waveform



8.3 Analog video signal characteristics

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
Video signal amplitude (VA, VB, VC)	V_{IAC}	-	3.81	-	V
	V_{IDC}	-	2.385	-	V

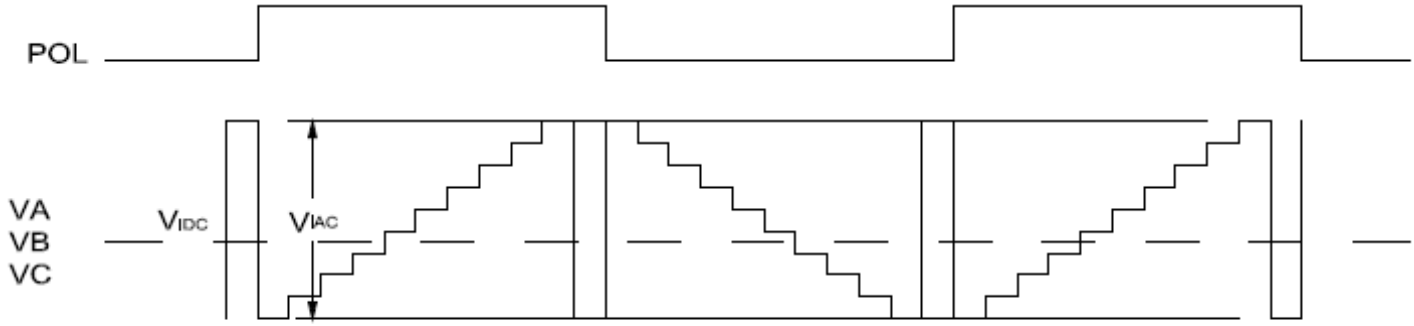
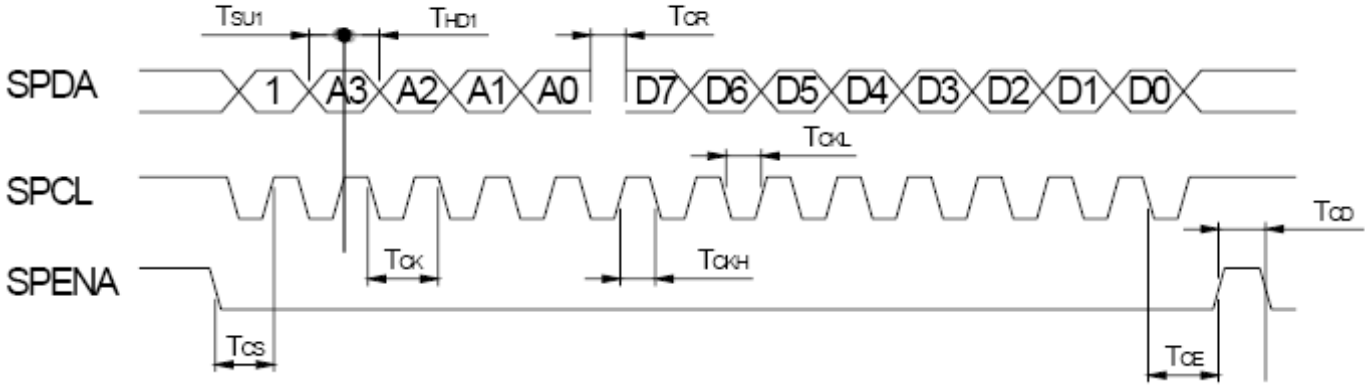


Fig. 4-(a) Horizontal timing

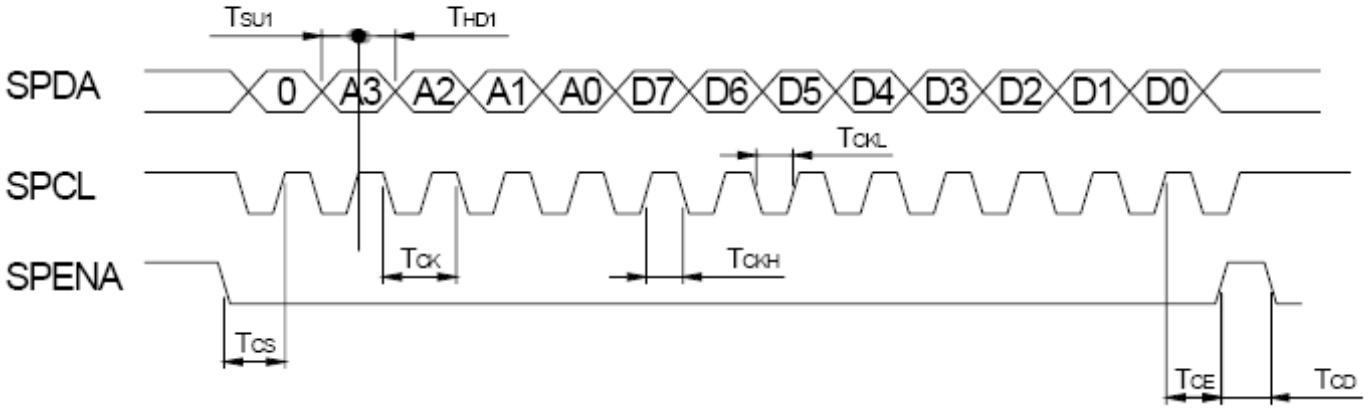
8.4 SPI timing characteristics

PARAMETER	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**
SPCL period	TCK	60	-	-	ns
SPCL high width	TCKH	30	-	-	ns
SPCL low width	TCKL	30	-	-	ns
Data setup time	TSU1	12	-	-	ns
Data hold time	THD1	12	-	-	ns
CS to SPCK setup time	TCS	20	-	-	ns
CS to SPDA hold time	TCE	20	-	-	ns
CS high pulse width	TCD	50	-	-	ns
SDI output latency	TCR		1/2	-	TCK

● SPI "read" timing

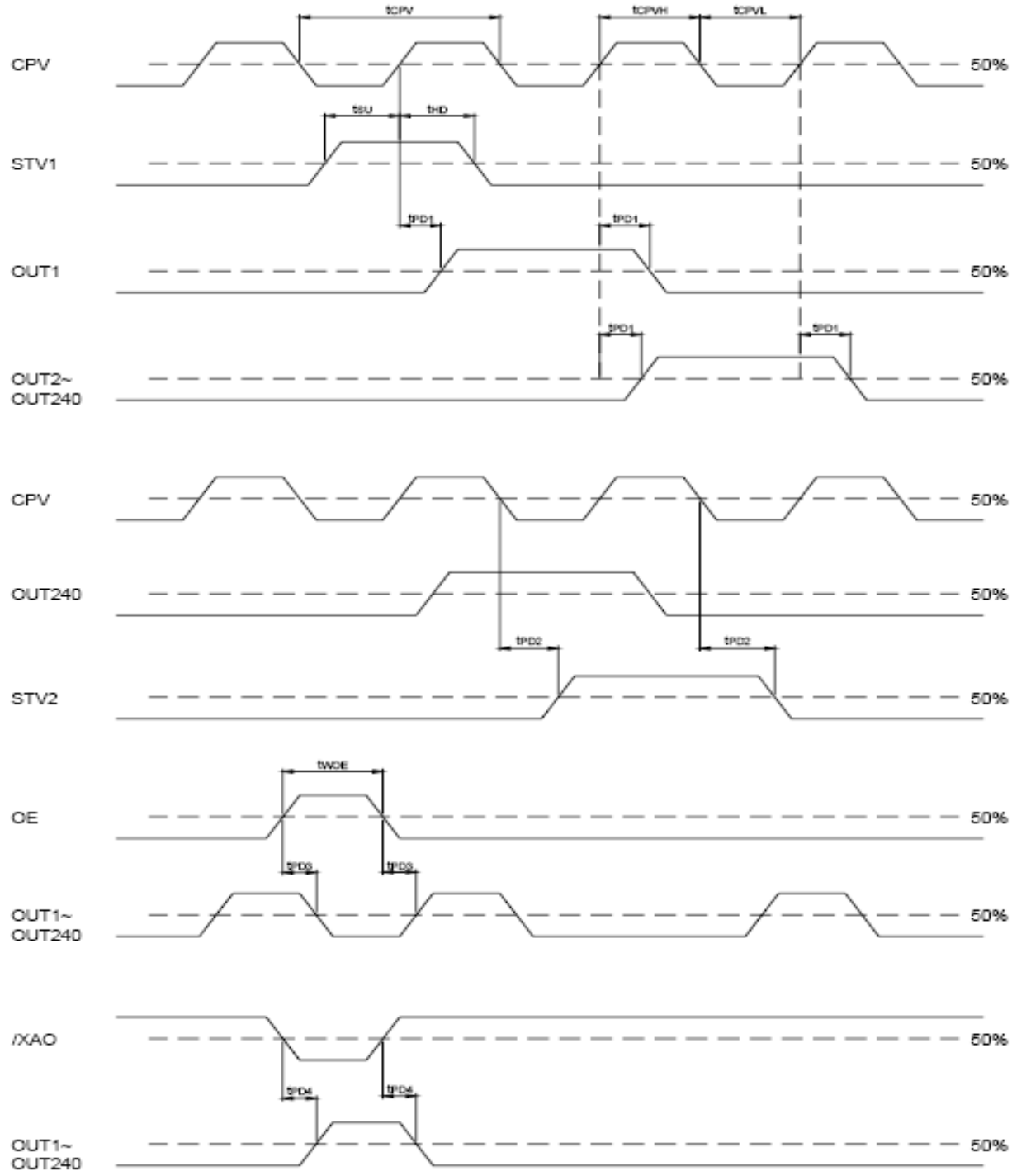


● SPI "write" timing



8.5 Gate Driver Timing Chart

PARAMETER	**Symbol**	**Condition**	Spec		**Unit**
			Min.	**Max.**	
Operation frequency	tCPV	-	5	-	μs
CPV pulse width	tCPVH,tCPVL	50%duty cycle	2.5	-	
OE pulse width	twOE		1	-	
Data setup time	tsu		0.4	-	ns
Data hold time	thd		0.7	-	
Output delay time	Tpd1	CL=300pF	-	1	
Output delay time	Tpd2	CL=300pF	-	0.8	
Output delay time	Tpd3	CL=300pF	-	0.8	
Output delay time	Tpd4	CL=300pF	-	10	



9. Optical Characteristics

Ta = 25±2℃ , ILED=140Ma

Item	Symbol	Condition	Min	Typ	Max	Unit	Note
Response time	Tr	θ=0°	-	15	30	ms	Note 3,5
	Tf		-	35	50	ms	
Contrast ratio	CR	At optimized	150	200	-		Note 4,5

			Viewing angle					
Color Chromaticity	White	Wx	θ=0°	0.25	0.30	0.35		Note 2,6,7
		Wy		0.27	0.32	0.37		
Viewing Angle	Hor	ΘR	CR≧10	-	(60)	-	Degree	Note 1
		ΘL		-	(60)	-		
	Ver	ΘT		-	(40)	-		
		ΘB		-	(60)	-		
Uniformity		U	-	(70)	(75)	-	%	Note 8
Brightness		-	-	-	300	-	cd/m2	Center of display

Note 1: Definition of viewing angle range

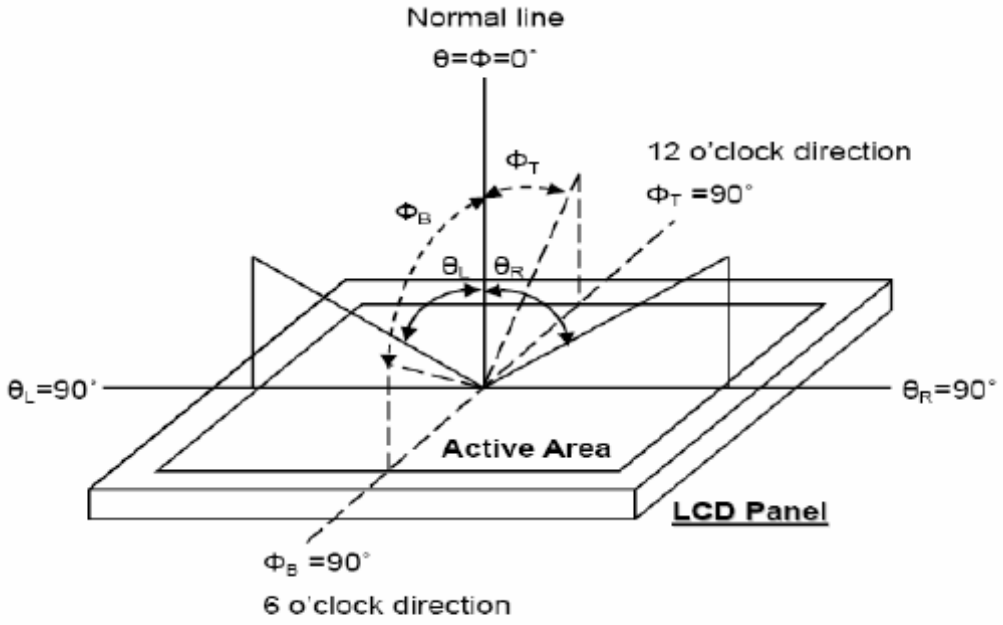


Fig. 8-1 Definition of viewing angle

Note 2: Test equipment setup:

After stabilizing and leaving the panel alone at a driven temperature for 5 minutes, the measurement should be executed. Measurement should be executed in a stable, windless, and dark room. Optical specifications are measured by Topcon BM-7 luminance meter 1.0° field of view at a distance of 50cm and normal direction.

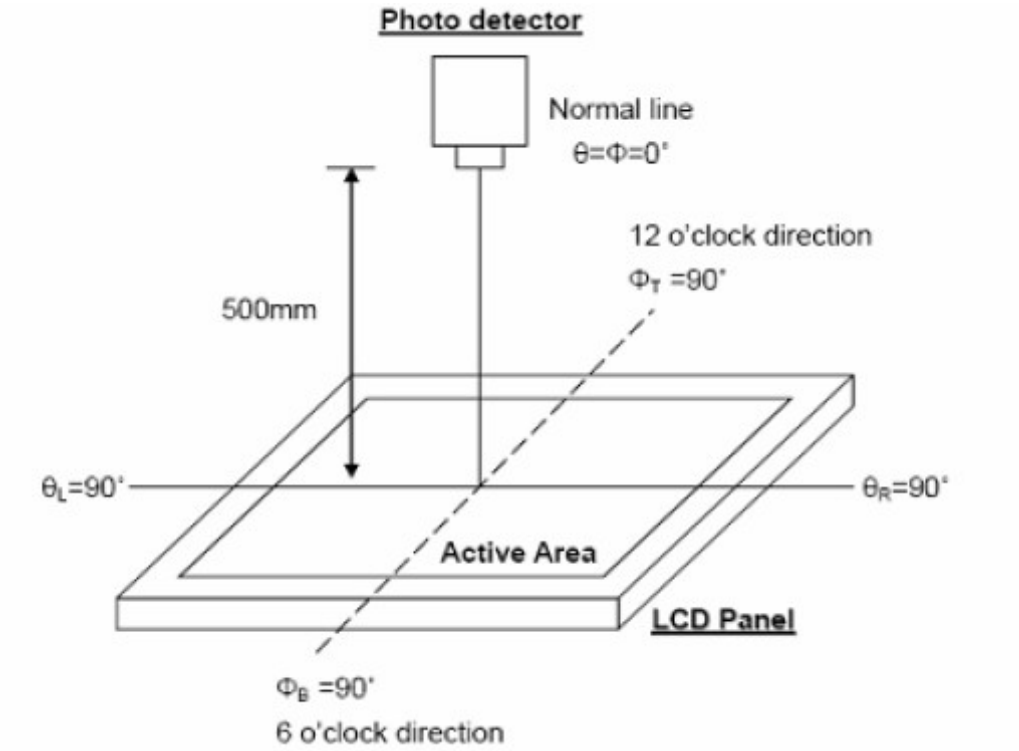


Fig. 8-2 Optical measurement system setup

Note 3: Definition of Response time:

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time, Tr, is the time between photo detector output intensity changed from 90% to 10%. And fall time, Tf, is the time between photo detector output intensity changed from 10% to 90%.

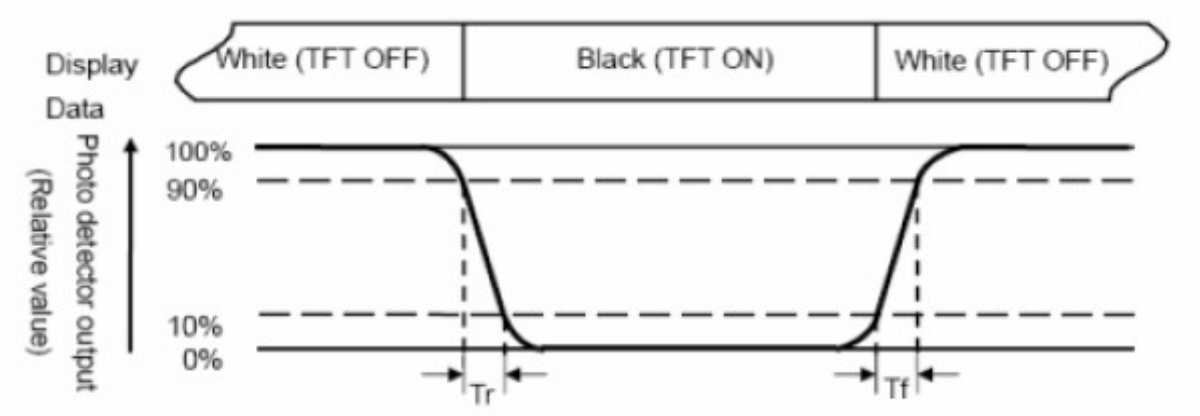


Fig. 3-3 Definition of response time

Note 4: Definition of contrast ratio:

The contrast ration is defined as the following expression.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Luminance measured when LCD on the “Black” state

Note 5: White Vi = Vi50 ± 1.5V

Black Vi = Vi50 ± 2.0V

“±” means that the analog input signal swings in phase with VCOM signal.

“±” means that the analog input signal swings out of phase with VCOM signal.

The 100% transmission is defined as the transmission of LCD panel when all the input terminals of Module are electrically opened.

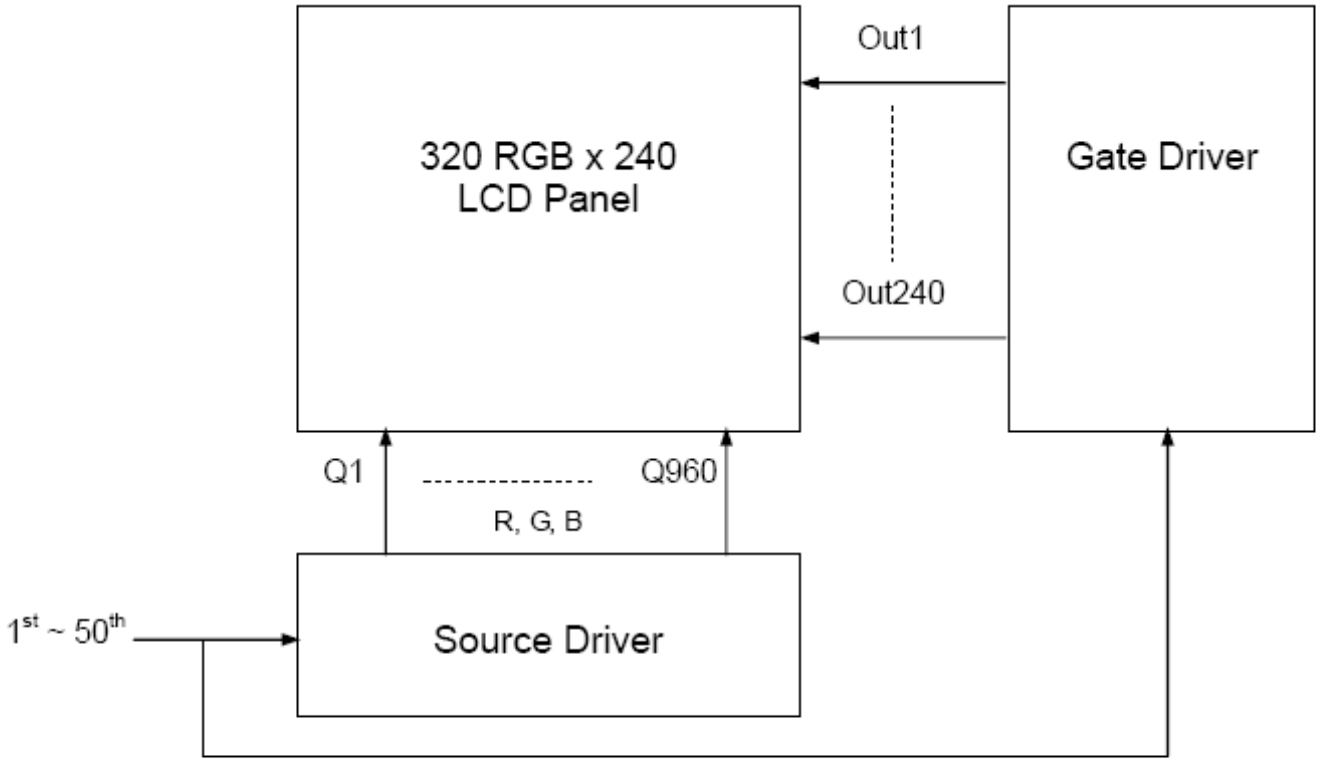
Note 6: Definition of color chromaticity (CIE 1931)

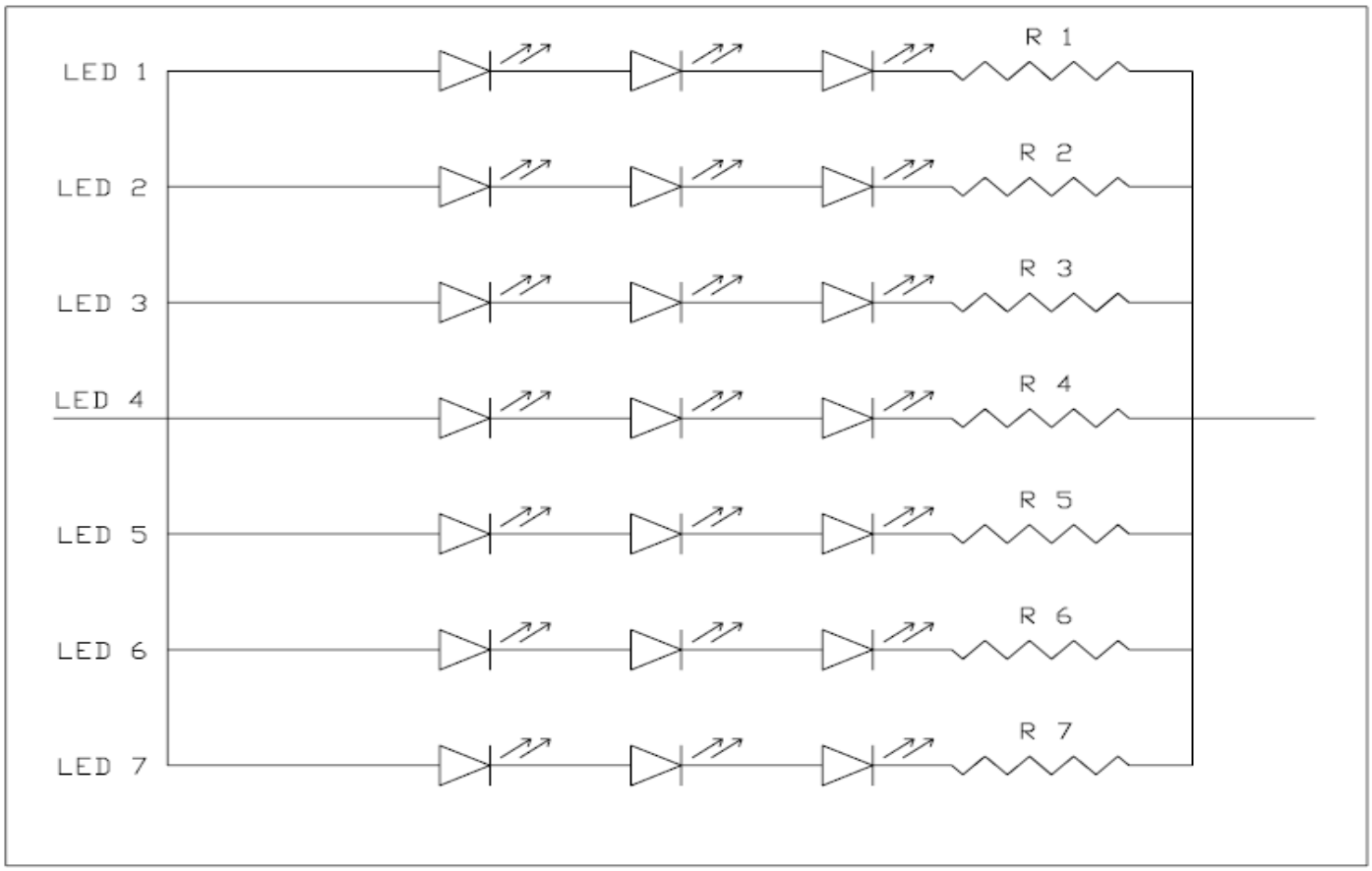
Color coordinates measured at the center point of LCD

Note 7: Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

$$\text{Note 8: Uniformity (U)} = \frac{\text{Brightness (min)}}{\text{Brightness (max)}} \times 100\%$$

10. BLOCK DIAGRAM





11. Input / Output Terminals

11.1 LCM PIN Definition

Pin No.	Symbol	I/O	Description
1	DGND	I	GROUND
2	+3.3V	I	Digital power: 3V~3.6V
3	+3.3V	0	Digital power: 3V~3.6V
4	DGND	I	GROUND
5	VGL	I	Gate off power
6	DGND	I	GROUND
7	VGL	I/O	Gate off power
8	DGND	I	GROUND
9	UD	I	Up/Down scan setting. H: Reverse scan / L: Normal scan
10	LR	I	Shift direction of device internal shift register control.
11	SPENA	I	Chip select
12	SPCK	I	Serial Clock
13	SPDA	I	Serial Data
14	POL	O	Polarity Signal connect to VCOM driving circuit.
15	DGND	I	GROUND
16	B5	I	Blue Data bit (MSB)
17	B4	I	Blue Data bit
18	B3	I	Blue Data bit
19	B2	I	Blue Data bit
20	B1	I	Blue Data bit
21	B0		Blue Data bit(LSB)
22	TOP	I	Terminal Resistance
23	RIGHT	I	Terminal Resistance
24	DGND	I	GROUND
25	G5	I	Green Data bit(MSB)
26	G4	I	Green Data bit
27	G3	I	Green Data bit
28	G2	I	Green Data bit
29	G1	I	Green Data bit
30	G0	I	Green Data bit(LSB)
31	BOTTOM	I	Terminal Resistance
32	LEFT	I	Terminal Resistance
33	AGND	I	Analog GROUND
34	+5V	I	Analog power: 4.5V~5.5V
35	+5V	I	Analog power: 4.5V~5.5V
36	AGND	I	Analog GROUND
37	R5	I	Red Data bit (MSB)
38	R4	I	Red Data bit
39	R3	O	Red Data bit
40	R2	I	Red Data bit
41	R1	I	Red Data bit
42	R0	I	Red Data bit(LSB)
43	DGND	I	GROUND
44	DGND	I	GROUND
45	DE	I	Data enable input.Normally pull low.
46	CLK	I	Dot data clock
47	HS	I	Horizontal synchronous signal
48	VS	I	Vertical synchronous signal
49	VCOM	I	VCOM driving input
50	DGND	I	GROUND

Note: 1. Control the input data format.

IF2,IF1	**Input data format**

L,L(default)	Serial RGB
L,H	Parallel RGB
H,L	CCIR601
H,H	CCIR656

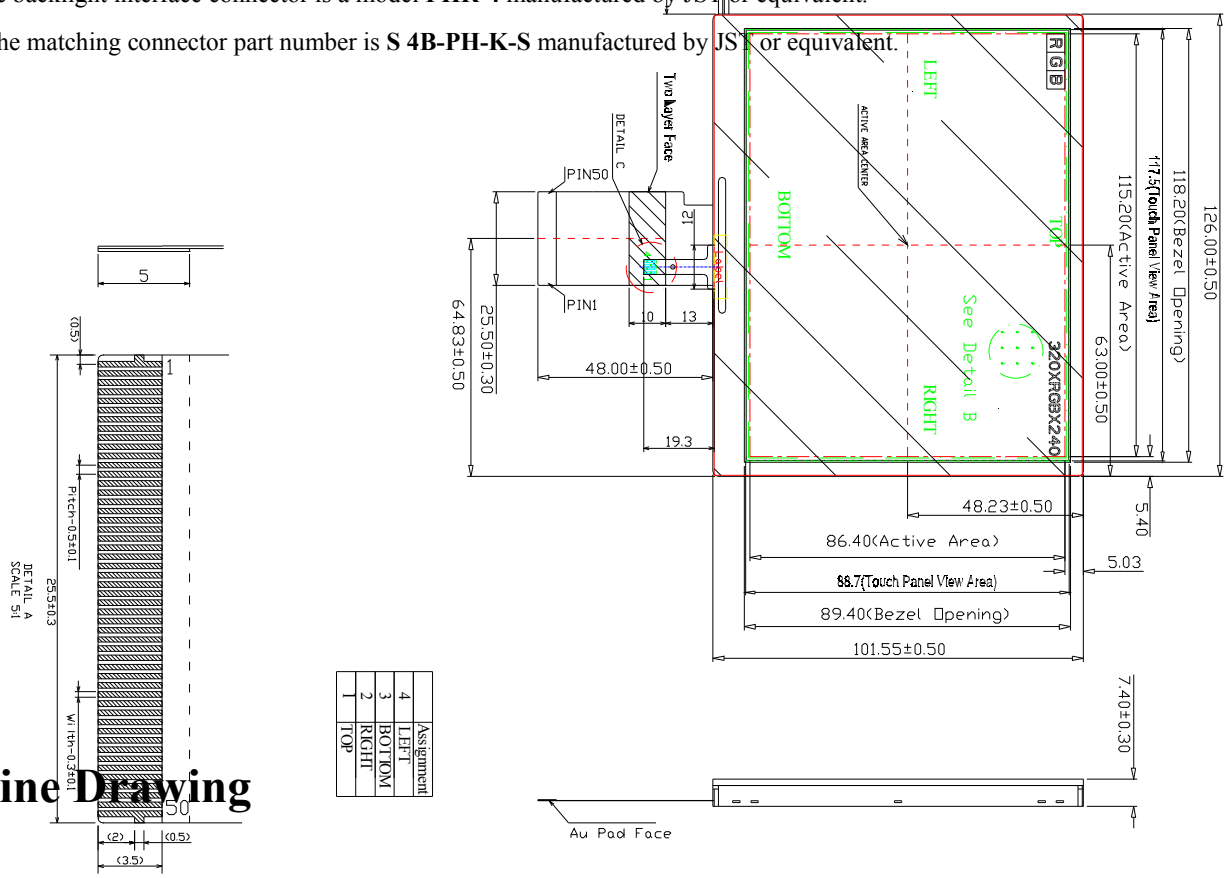
11.2. Backlight PIN Definition

Pin No.	Symbol	I/O	Description
1	LED +	I	LED_Anode (13.2Vdc when ILED=20mA)
2	LED -	I	LED_Cathode

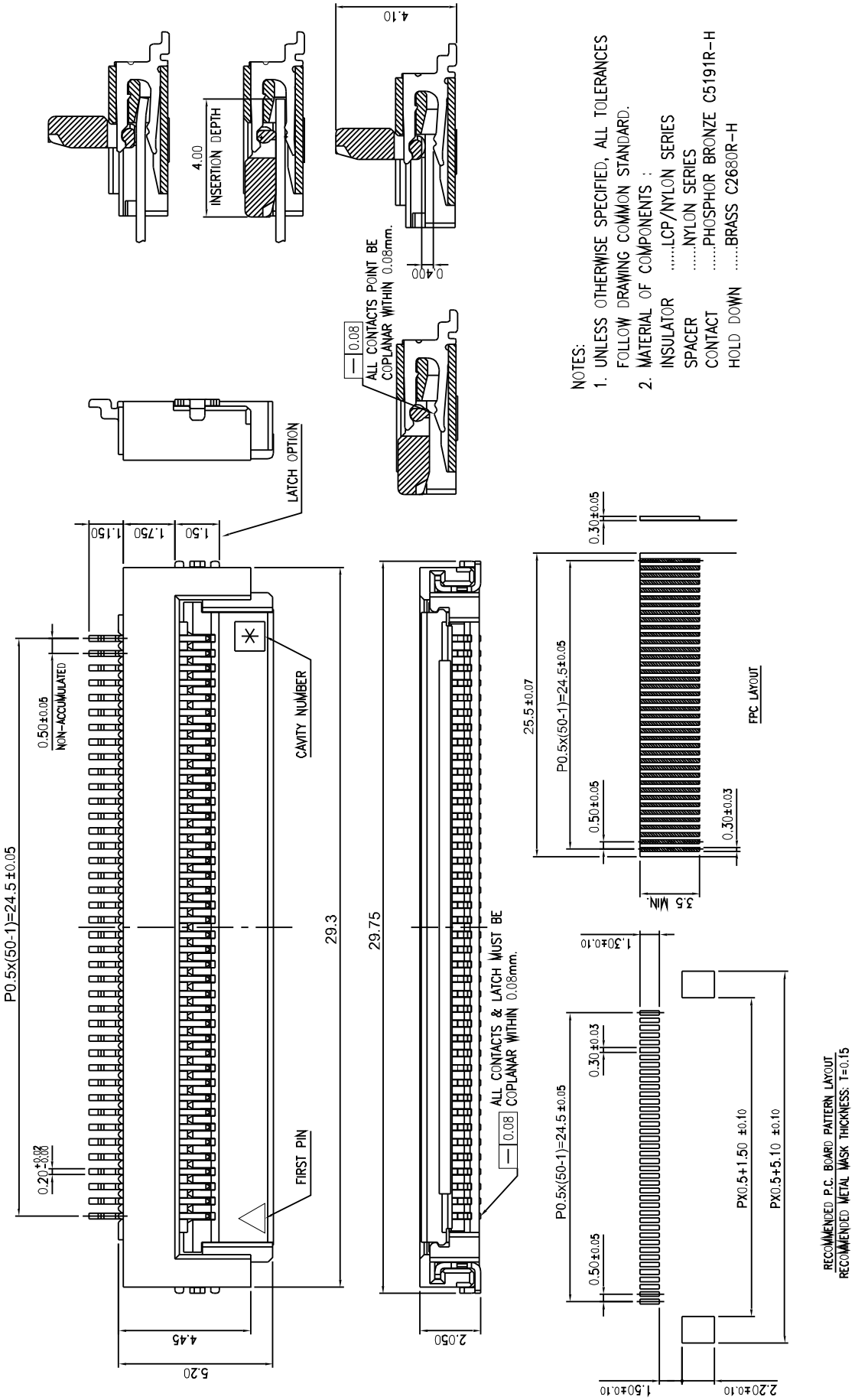
Note: The backlight interface connector is a model **PHR-4** manufactured by JST or equivalent.

The matching connector part number is **S 4B-PH-K-S** manufactured by JST or equivalent.

12. Outline Drawing



CONNECT DRAWING:



13. Quality Assurance

No.	Test Items	Test Condition	REMARK

1	High Temperature Storage Test	Ta=70℃ 240h	
2	Low Temperature Storage Test	Ta=-20℃ 240h	
3	High Temperature Operation Test	Ta=60℃ 240h	
4	Low Temperature Operation Test	Ta=-10℃ 240h	
5	High Temperature and High Humidity Operation Test	Ta=60℃ 90%RH 240h	
6	Electro Static Discharge Test	-Panel Surface/Top_Case: 150pF ±15kV 150Ω (direct discharge, five times) -FPC input terminal : 100pF ±200V 0Ω	
7	Shock Test (non-operating)	Half sine wave, 180G, 2ms one shock of each six faces (I.e. run 180G 2ms for all six faces)	
8	Vibration Test (non-operating)	Sine wave, 10 ~ 500 ~ 10Hz, 1.5G, 0.37oct/min 3 axis, 1hour/axis	
9	Thermal Shock Test	-20℃(0.5h) ~70℃(0.5h) / 100 cycles	

***** Ta= Ambient Temperature

14. Designation of Lot Mark

14-1. Lot Mark

A	B	C	D	E	F	G	H	I	J	K	L

A : YEAR B,C : MONTH

D : WEEK E,F : PRODUCTION MANAGEMENT

G,H,I,J,K : SERIAL NO.

Note

1. YEAR

Year	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012
Mark	3	4	5	6	7	8	9	0	1	2

2. MONTH

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Mark	01	02	03	04	05	06	07	08	09	10	11	12

3. WEEK

Week	1st~7th	8th~14th	15th~21st	22nd~28th	29th~31st
Mark	1	2	3	4	5

4. SERIAL NO.

Year	1~999999	1000000~
Mark	000001~999999	A00000~A99999, ……..,Z99999

14-2. Location of Lot Mark

Serial NO. is printed on the label. The label is attached to the backside of the LCD module. This is subject to change without prior notice.