

SPECIFICATIONS

CUSTOMER : _____

SAMPLE CODE : GFG128064I-YPFE-05

DRAWING NO. : _____

DATE : 2011.04.29

CERTIFICATION : ROHS

Customer Sign	Sales Sign	Approved By	Prepared By

Revision Record

Data(y/m/d)	Ver.	Description	Note	page
2011.04.29	00	New		17

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1. SCOPE

This specification covers the engineering requirements for the GFG128064I-YPFE-05 liquid crystal module.

2. PRODUCT SPECIFICATIONS

2.1 General

- 128 \diamond 64 dot matrix LCD
- STN (Y/G) , Positive mode LCD panel
- Transflective , Wide temperature type
- 6 o'clock
- Back light: Edge LED (white)
- Multiplexing driving : 1/65duty, 1/9bias

- Controller IC
ST7565

Item	Characteristic
Dot configuration	128 \diamond 64
Dot dimensions(mm)	0.48 \diamond 0.48
Dot spacing (mm)	0.52 \diamond 0.52
Module dimensions (Horizontal \diamond Vertical \diamond Thickness, mm)	80 \diamond 54 \diamond 9.7 max.
Viewing area (Horizontal \diamond Vertical, mm)	70.7 \diamond 38.8
Active area (Horizontal \diamond Vertical, mm)	66.52 \diamond 33.24

2.2 Mechanical Characteristics

V_{OPR} : Operating voltage

f_{FRM} : Frame frequency

t_{ON} : Response time (rise)

t_{OFF} : Response time (fall)

2.7 LED Back-light Characteristics

2.7.1 Electrical / optical specifications

$T_a = 25^\circ\text{C}$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Forward voltage	V_f	$I_f=60\text{mA}$, White	2.9	3.2	3.6	V
LED *Luminous Intensity	I_v	$I_f=60\text{mA}$, White	--	150	--	Cd/m ²
Chromaticity Coordinate	x	$I_f=60\text{mA}$, White	0.26	0.31	0.36	
	y		0.25	0.32	0.37	
Reverse Current	I_R	$V_R=5\text{V}$, White	--	--	0.1	mA

Note: * Measured at the bare LED back-light unit.

2.7.2 LED Maximum Operating Range

Item	Symbol	White	Unit
Power Dissipation	P_{AD}	288	mW
Forward Current	I_f	80	mA
Reverse Voltage	V_R	5	V

3. RELIABILITY

3.1 Reliability

Test item	Test condition	Evaluation and assessment
Operation at high temperature and humidity	40 °C \pm 2 °C 90%RH for 500hours	No abnormalities in functions* and appearance**
Operation at high temperature	60 °C \pm 2 °C for 500 hours	No abnormalities in functions* and appearance**
Heat shock	-20 ϕ ~ +60 °C Left for 1 hour at each temperature, transition time 5 min, repeated 10times	No abnormalities in functions* and appearance**
Low temperature	-20 \pm 2 °C for 500 hours	No abnormalities in functions* and appearance**
Vibration	Sweep for 1 min at 10 Hz, 55Hz, 10Hz, amplitude 1.5mm 2 hrs each in the X,Y and Z directions	No abnormalities in functions* and appearance**
Drop shock	Dropped onto a board from a height of 10cm	No abnormalities in functions* and appearance**

* Dissipation current, contrast and display functions

** Polarizing filter deterioration, other appearance defects

3.2 Liquid crystal panel service life

100,000 hours minimum at 25 °C \pm 10 °C

3.3 definition of panel service life

- Contrast becomes 30% of initial value
- Current consumption becomes three times higher than initial value
- Remarkable alignment deterioration occurs in LCD cell layer
- Unusual operation occurs in display functions

4. OPERATING INSTRUCTIONS

4.1 Input signal Function

Pin No	Symbol	I/O	Function
1	/CS1	I	This is the chip select signal. When CS1 = "L" and CS2 = "H," then the chip select becomes active, and data/command I/O is enabled.
2	/RES	I	When RES is set to "L," the settings are initialized. The reset operation is performed by the RES signal level.
3	A0	I	This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command. A0 = "H": Indicates that D0 to D7 are display data. A0 = "L": Indicates that D0 to D7 are control data.
4	WR(R/W)	I	<ul style="list-style-type: none"> When connected to an 8080 MPU, this is active LOW. (R/W) This terminal connects to the 8080 MPU WR signal. The signals on the data bus are latched at the rising edge of the WR signal. <ul style="list-style-type: none"> When connected to a 6800 Series MPU: This is the read/write control signal input terminal. When R/W = "H": Read. When R/W = "L": Write.
5	RD(E)	I	<ul style="list-style-type: none"> When connected to an 8080 MPU, this is active LOW. (E) This pin is connected to the RD signal of the 8080 MPU, and the ST7565S series data bus is in an output status when this signal is "L". <ul style="list-style-type: none"> When connected to a 6800 Series MPU, this is active HIGH. This is the 6800 Series MPU enable clock input terminal.
6~13	D0 to D5 D6 (SCL) D7 (SI)	I/O	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected (P/S = "L") : D0 to D5 are set to high impedance. D6 : the serial clock input (SCL) ; D7 : serial data input (SI) . When the chip select is not active, D0 to D7 are set to high impedance.
14	VDD	PS	Shared with the MPU power supply terminal Vcc.
15	VSS	PS	This is a 0V terminal connected to the system GND.
16	VOUT	O	DC/DC voltage converter. Connect a capacitor between this terminal and VSS.
17	CAP5-	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal.
18	CAP3-	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal.
19	CAP1+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.
20	CAP1-	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal.

21	CAP2-	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2+ terminal.															
22	CAP2+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.															
23	CAP4-	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2+ terminal.															
24	VRS	PS	This is the internal-output VREG power supply for the LCD power supply voltage regulator.															
25~29	V1,V2, V3,V4, V5	PS	This is a multi-level power supply for the liquid crystal drive. The voltage Supply applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divided or through changing the impedance using an op.amp. Voltage levels are determined based on VDD, and must maintain the relative magnitudes shown below. VDD (= V0) ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ V5															
30	VR	I	Output voltage regulator terminal. Provides the voltage between VDD and V5 through a resistive voltage divider. IRS = "L" : the V5 voltage regulator internal resistors are not used . IRS = "H" : the V5 voltage regulator internal resistors are used .															
31	C86	I	This is the MPU interface switch terminal. C86 = "H": 6800 Series MPU interface. C86 = "L": 8080 MPU interface.															
32	P/S	I	This is the parallel data input/serial data input switch terminal. P/S = "H": Parallel data input. P/S = "L": Serial data input. The following applies depending on the P/S status: <table border="1" data-bbox="475 1285 1370 1529"> <thead> <tr> <th>P/S</th> <th>Data/Comman</th> <th>Data</th> <th>Read/Write</th> <th>Serial Clock</th> </tr> </thead> <tbody> <tr> <td>"H"</td> <td>A0</td> <td>D0 to D7</td> <td>RD, WR</td> <td>X</td> </tr> <tr> <td>"L"</td> <td>A0</td> <td>SI (D7)</td> <td>Write only</td> <td>SCL (D6)</td> </tr> </tbody> </table> When P/S = "L", D0 to D5 may be "H", "L" or Open. RD (E) and WR (R/W) are fixed to either "H" or "L". With serial data input, It is impossible read data from RAM .	P/S	Data/Comman	Data	Read/Write	Serial Clock	"H"	A0	D0 to D7	RD, WR	X	"L"	A0	SI (D7)	Write only	SCL (D6)
P/S	Data/Comman	Data	Read/Write	Serial Clock														
"H"	A0	D0 to D7	RD, WR	X														
"L"	A0	SI (D7)	Write only	SCL (D6)														
33	/HPM	I	This is the power control terminal for the power supply circuit for liquid crystal drive. /HPM = "H": Normal mode /HPM = "L": High power mode															
34	IRS	I	This terminal selects the resistors for the V5 voltage level adjustment. IRS = "H": Use the internal resistors IRS = "L": Do not use the internal resistors. The V5 voltage level is regulated by an external resistive voltage divider attached to the VR terminal															

Table 1

P/S	/CS1	CS2	A0	/RD	/WR	C86	D7	D6	D5~D0
H: Parallel Input	/CS1	CS2	A0	/RD	/WR	C86	D7	D6	D5~D0
L: Serial Input	/CS1	CS2	A0	—	—	—	SI	SCL	(HZ)

“—” indicates fixed to either “H” or to “L”

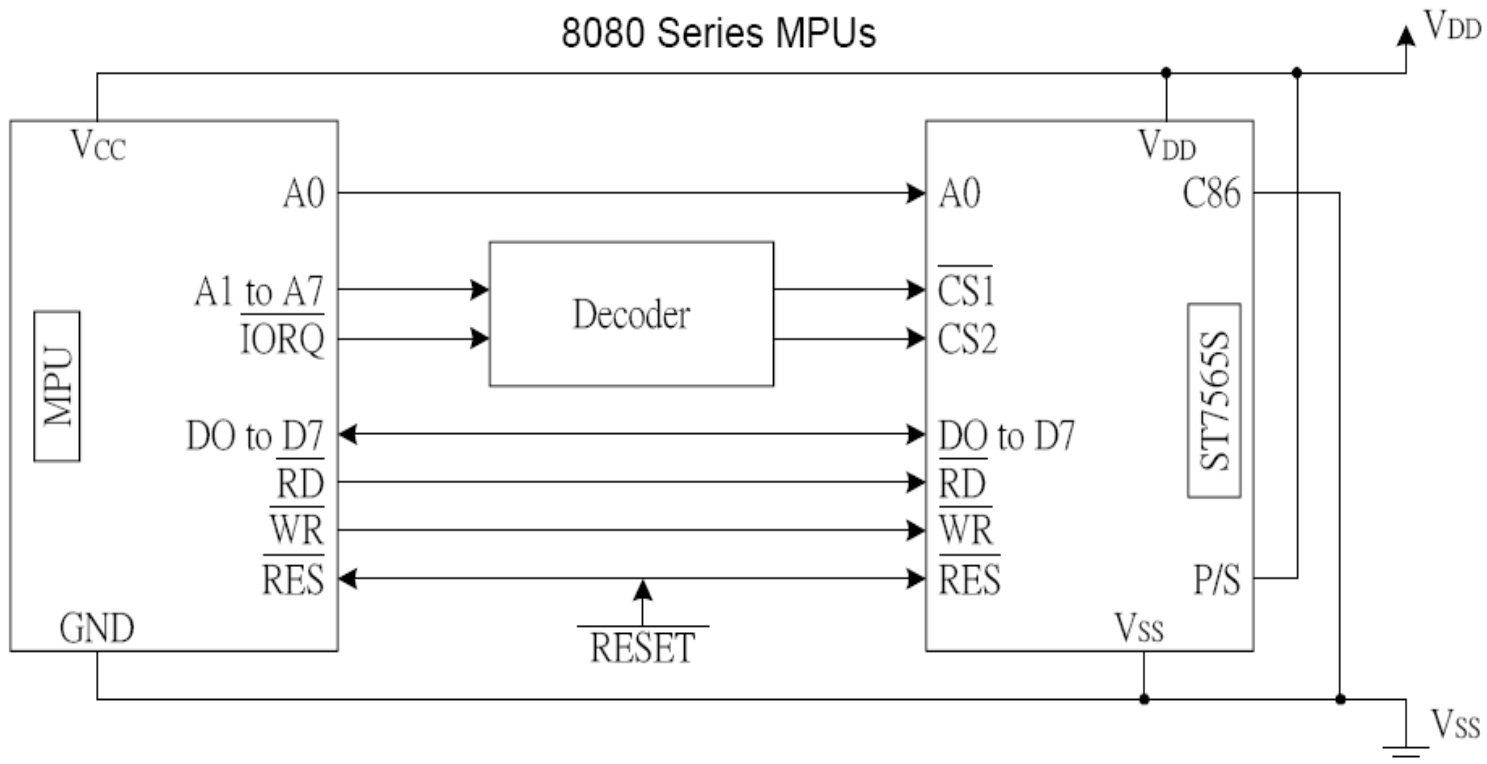
Table 2

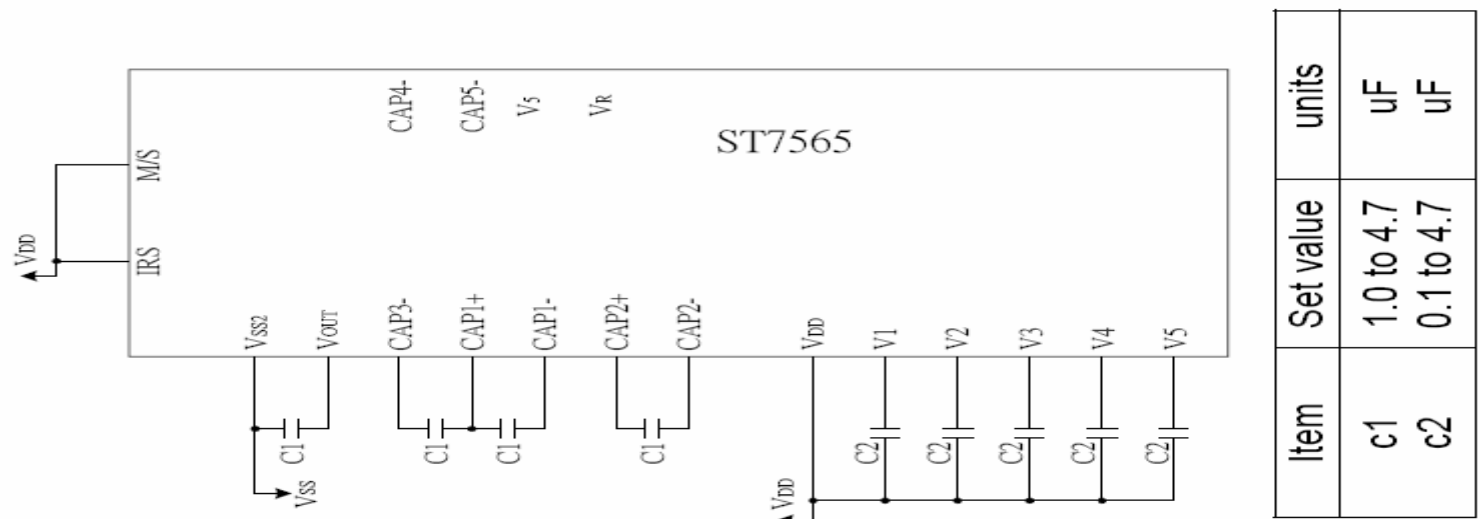
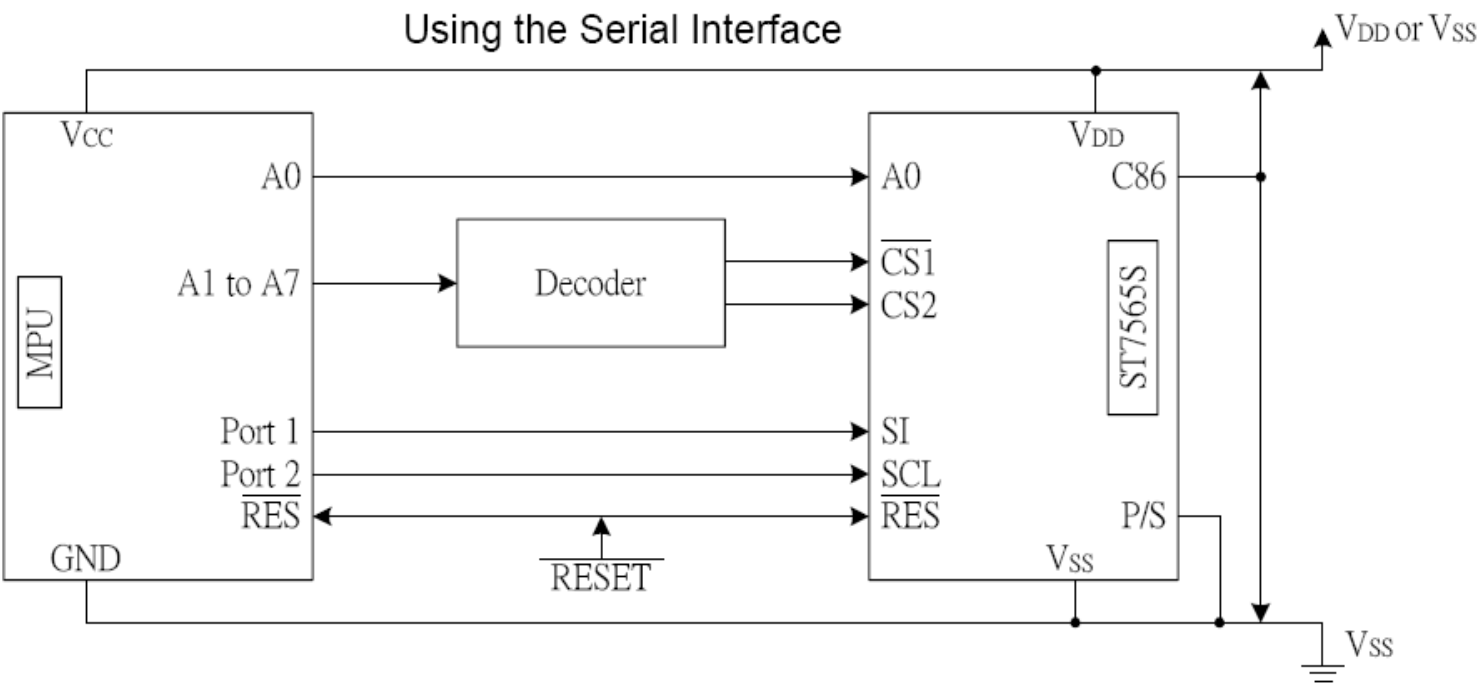
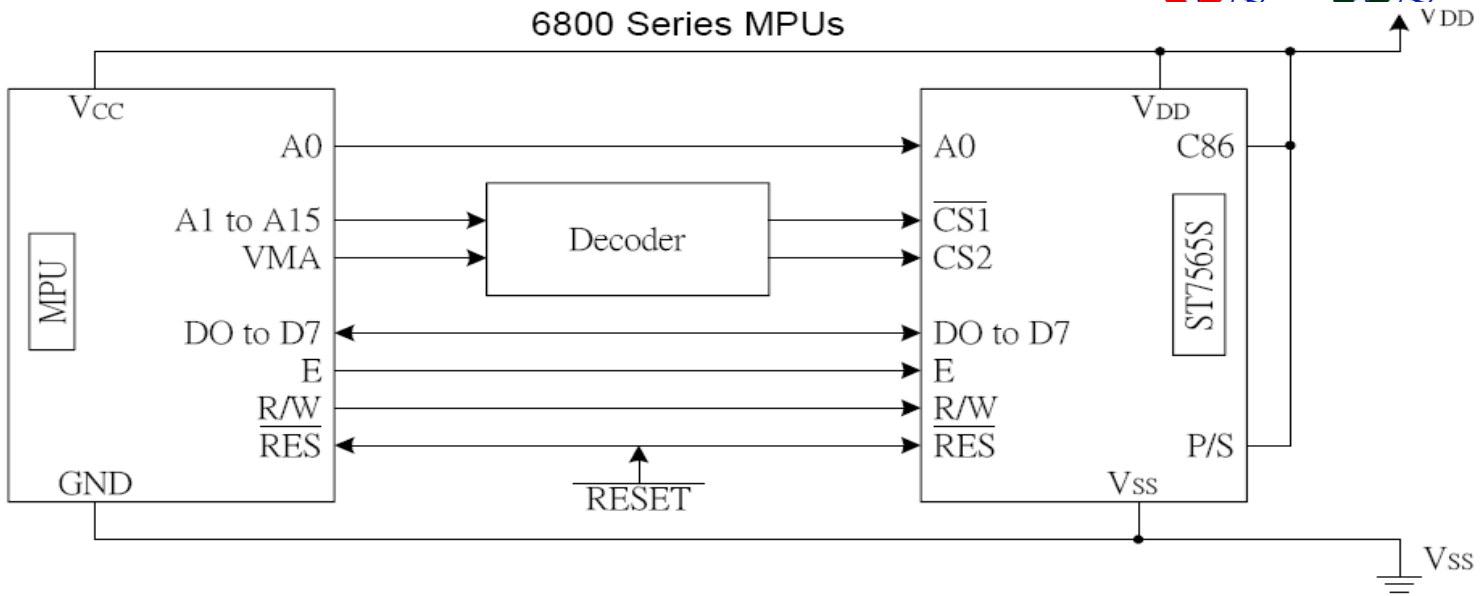
C86 (P/S=H)	/CS1	CS2	A0	E(/RD)	R/W(/WR)	D7~D0
H: 6800 Series	/CS1	CS2	A0	E	R/W	D7~D0
L: 8080 Series	/CS1	CS2	A0	/RD	/WR	D7~D0

Table 3

Shared	6800 Series	8080 Series		Function
	R/W	/RD	/WR	
A0				
1	1	0	1	Reads the display data
1	0	1	0	Writes the display data
0	1	0	1	Status read
0	0	1	0	Write control data (command)

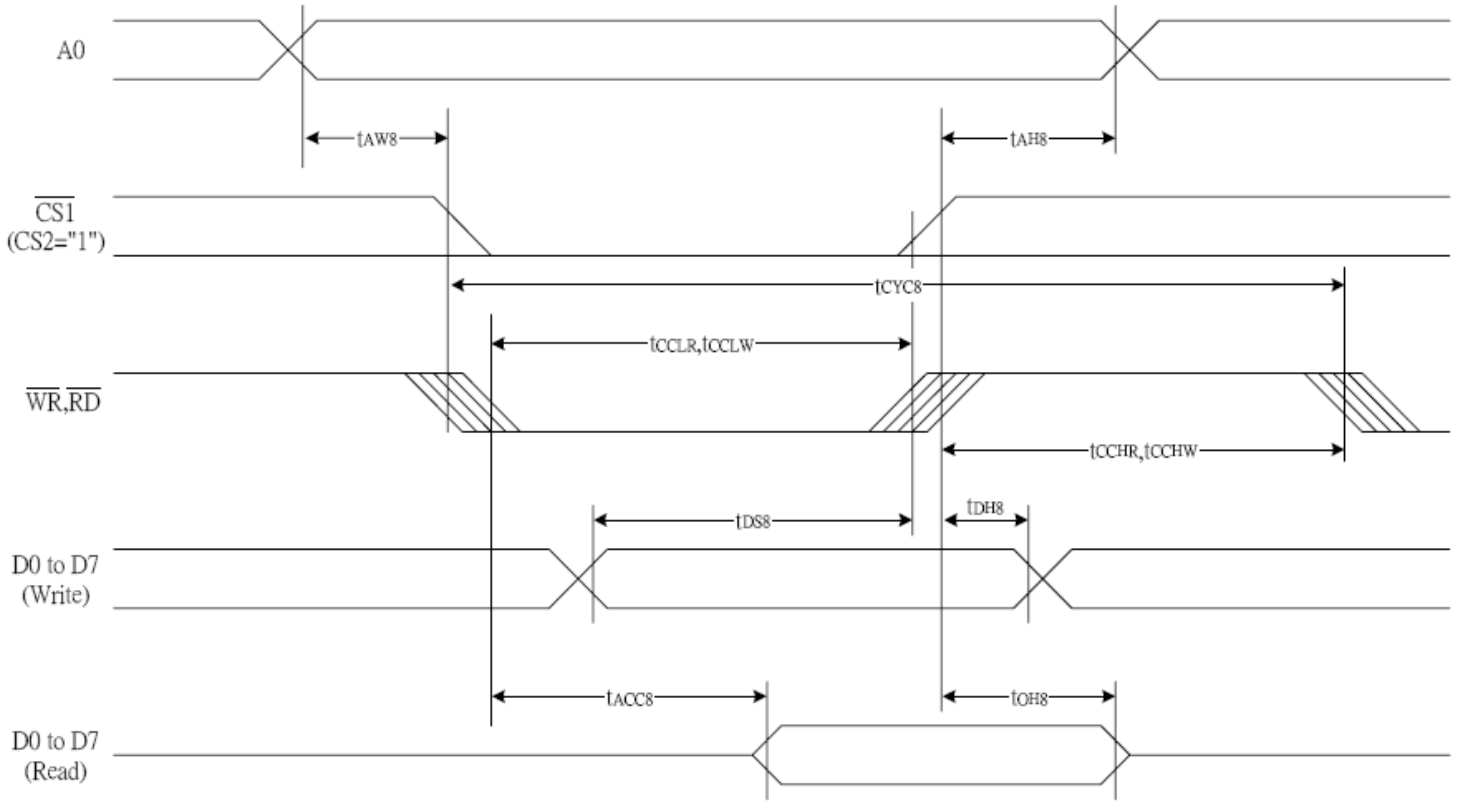
4.2 Voltage Generator Circuit





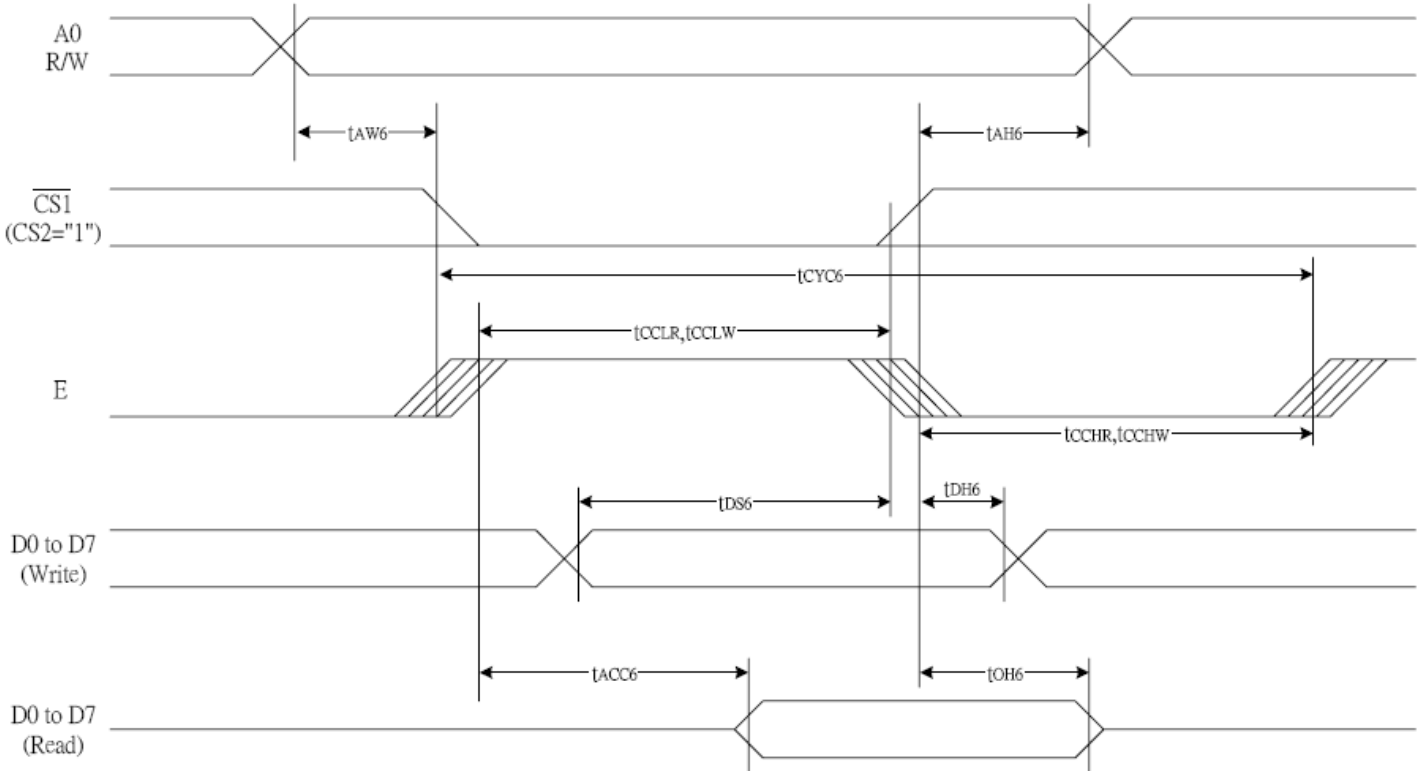
4.3 Timing Diagram

System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)



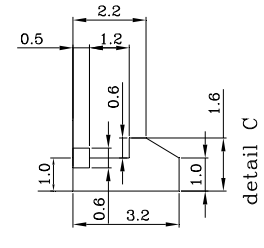
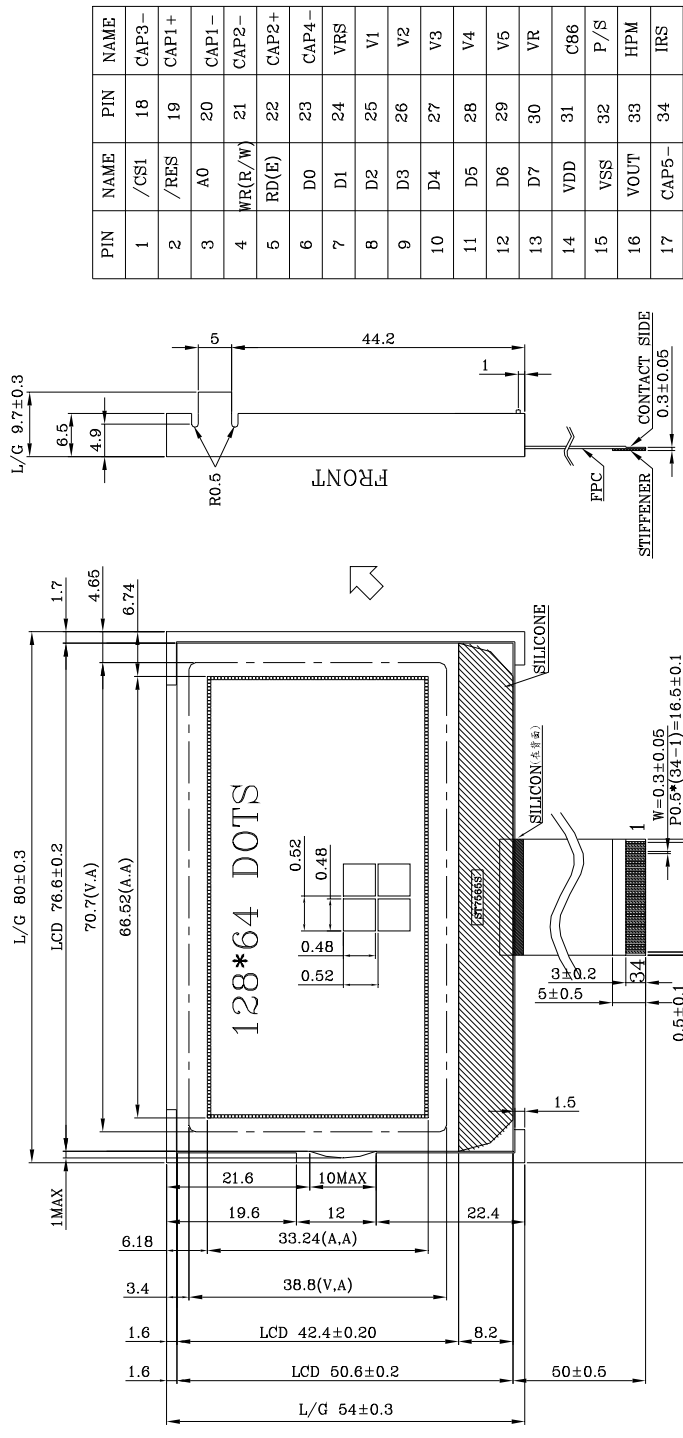
Item	Signal	Symbol	Condition	Rating		Units
				Min	Max.	
Address hold time	A0	t_{AH8}	--	0	--	ns
Address setup time	A0	t_{AW8}	--	0	--	ns
System cycle time	A0	t_{CYC8}	--	240		
Control L pulse width (WR)	WR	t_{CCLW}	--	80	--	ns
Control L pulse width (RD)	RD	t_{CCLR}	--	140	--	ns
Control H pulse width (WR)	WR	t_{CCHW}	--	80	--	ns
Control H pulse width (RD)	RD	t_{CCHR}	--	80	--	ns
RD access time	D0 to D7	t_{DS8}	--	40	--	ns
Output disable time		t_{DH8}	--	10	--	ns
		t_{ACC8}	$C_L=100pF$	--	70	ns
		t_{OH8}	$C_L=100pF$	5	50	ns

System Bus Read/Write Characteristics 2 (For the 6800 Series MPU)



Item	Signal	Symbol	Condition	Rating		Units
				Min	Max.	
Address hold time	A0	t_{AH8}	--	0	--	ns
Address setup time		t_{AW8}		0	--	ns
System cycle time	A0	t_{CYC8}	--	240		
Control L pulse width (WR)	WR	t_{CCLW}	--	80	--	ns
Control L pulse width (RD)	RD	t_{CCLR}		140	--	ns
Control H pulse width (WR)	WR	t_{CCHW}		80	--	ns
Control H pulse width (RD)	RD	t_{CCHR}		80	--	ns
RD access time	D0 to	t_{DS8}	--	40	--	ns
Output disable time	D7	t_{DH8}		10	--	ns
		t_{ACC8}	$C_L=100pF$	--	70	ns
		t_{OH8}		5	50	ns

ROHS



- NOTES:
1. DRIVE METHOD: 1/65DUTY, 1/9BIAS,VDD 3.3V, VOPI0.0V.
 2. VIEW ANGLE: 6 0'CLOCK.
 3. DISPLAY TYPE: STN(Y/G), TRANSPARENT/POSITIVE.
 4. OPERATING TEMP: -20 TO 70°C.
 5. STORAGE TEMP: -30 TO 80°C.
 6. CONNECTION:COG+FPC.(Small panel is on top layer)
 7. IC:ST7666S-G.
 8. 磨邊
 9. BACKLIGHT:WHITE(VF=3.2V)
 10. INTERFACE: 8 BITS, PARALLEL DATA INPUT FOR 8080.
 11. NOT DIMENSION TOLERANCES IS ±0.3.

修改内容

版本

日期